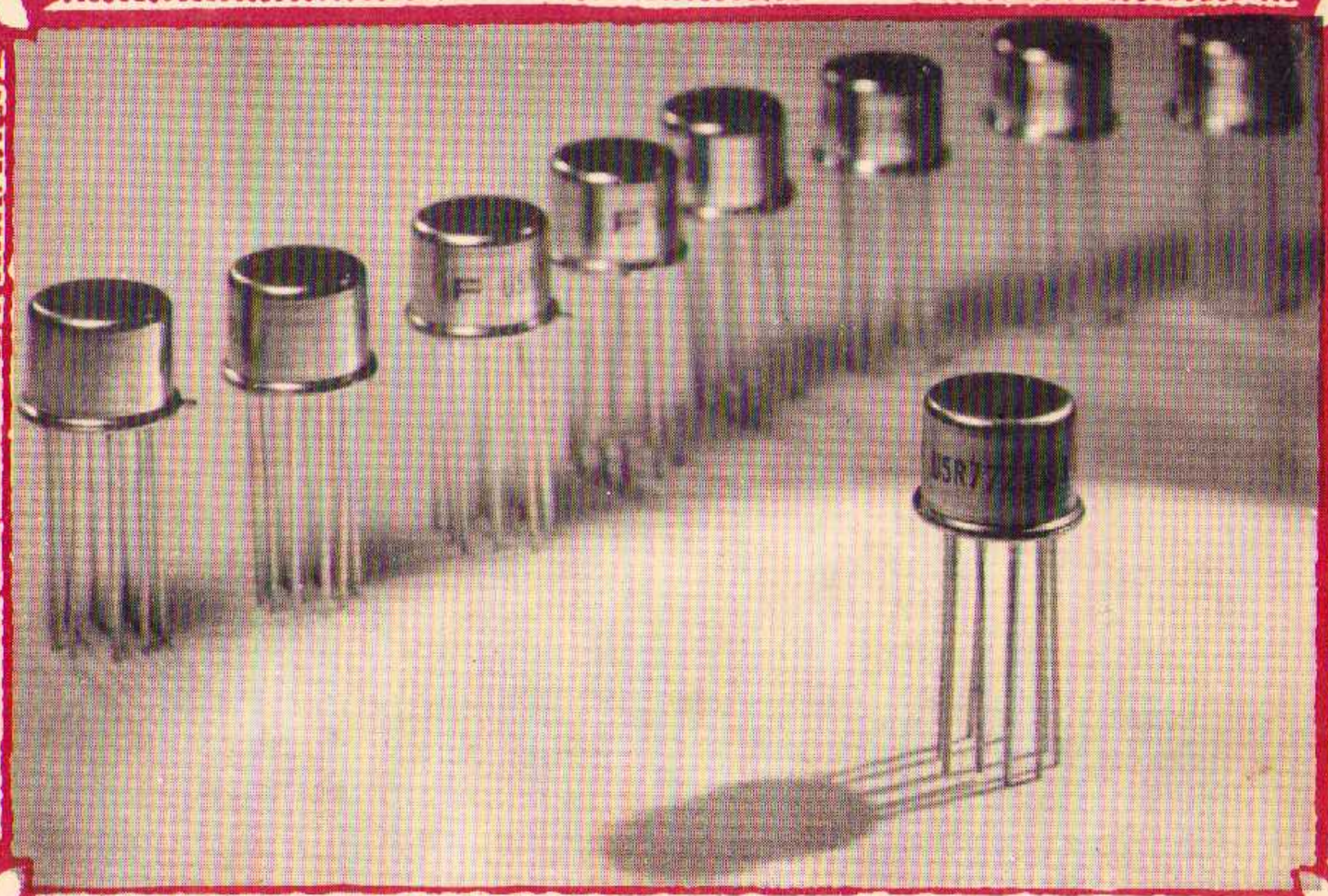
TECHNISCHE DOCUMENTATIE 1970

DEEL 1 2 3 4 5 6 7 8 9 **10** 11 12



voeding anno 1970

van oorn
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PRIJS *f* 1,30

Jaarabonnement: ƒ 10,40 bij vooruitbetaling op postgiro 295550 ten name van:
N.V. Technische Handelmaatschappij Van Dam Elektronica-Rotterdam.
Abonnementen gaan in per 1 januari 1970.

- -

VOOR leveringsvoorwaarden, doelstelling, abonnementen, verschijningsdata enz.
=== zie technische documentatie 1970 deel 1 t/m 4, pagina 2 en 3.

- -

ANTWOORDKAARTEN

Bij deze documentatie zijn verschillende antwoordkaarten gevoegd, waarvan bij bestellingen, verhuizing, nieuwe abonnementen enz. gebruik kan worden gemaakt. Door juiste invulling van deze kaarten kan een snelle service onzerzijds worden gegarandeerd. Wij verzoeken U vriendelijk deze kaarten met blokletters in te vullen en voldoende te frankeren.

- -

Inleiding. Coördinatie: Paul E. Annokkee

In de delen 7-9 hebben wij de prijslijst opgenomen van TTL IC's, welke in ons voorraadprogramma aanwezig waren; inmiddels heeft U naar aanleiding hiervan een nieuwe prijslijst toegezonden gekregen; uit de snelheid, waarmede prijsveranderingen kunnen optreden blijkt wel hoe moeilijk het is een prijscourant uit te brengen. Daarom is besloten aan onze abonnees van de uitgave "Technische Documentatie" 3 tot 4 keer per jaar een beknopt overzicht te zenden van voorraadtypen halfgeleiders, condensatoren, elco's, weerstanden, potmeters, cijferbuizen en andere belangrijke componenten. Teneinde een en ander te kunnen coördineren stellen wij het byzonder op prijs van U de achter in deze documentatie gevoegde enquètekaart ingevuld terug te mogen ontvangen. De reacties worden gebruikt bij het uitgeven van een catalogus in de loop van 1971.

In deze documentatie komen weer enkele nieuwe produkten aan de beurt; speciale aandacht is op zijn plaats voor de µA 723C spanningsregulator, waarvan op pag. 4 t/m 10 de technische gegevens en applicaties zijn opgenomen. Deze geïntegreerde schakeling maakt het mogelijk, voedingen te construeren vanaf + of - 3 volt tot maximaal + of - 250 volt . . . . Toch is de prijs hiervan niet hoog: zie hiervoor bijgevoegde losse prijslijst.

Verder in deze documentatie een toepassing van de dubbele 709 (SN72709DN); hierbij kan ook gebruik worden gemaakt van de 741 opamp: zie TD 1970 deel 1-4. Ook de comparators 710 en 711 (resp. SN 72710N en SN 72711N) zijn in deze uitgave opgenomen.

Op pagina 20 t/m 22 is een applicatie-voorbeeld opgenomen van TTL IC's voor een volwaardige digitale klok. Deze documentatie is een overdruk uit "Siemens-Bauteile Informationen 8 (Heft 4)". Volledigheidshalve geven wij U hierbij het algemene 7400 typenummer voor de gebruikte geïntegreerde schakelingen (zie ook onze vergelijkingstabellen in de delen 5-6 en 7-9).

FLH 101 (7400), FLJ 121 (7473), FLL 101 (74141), FLJ 161 (7490), FLJ 171 (7492).

Omslagfoto: Fotografie Dick Wolters - Rotterdam.

n.v. technische handelmaatschappij

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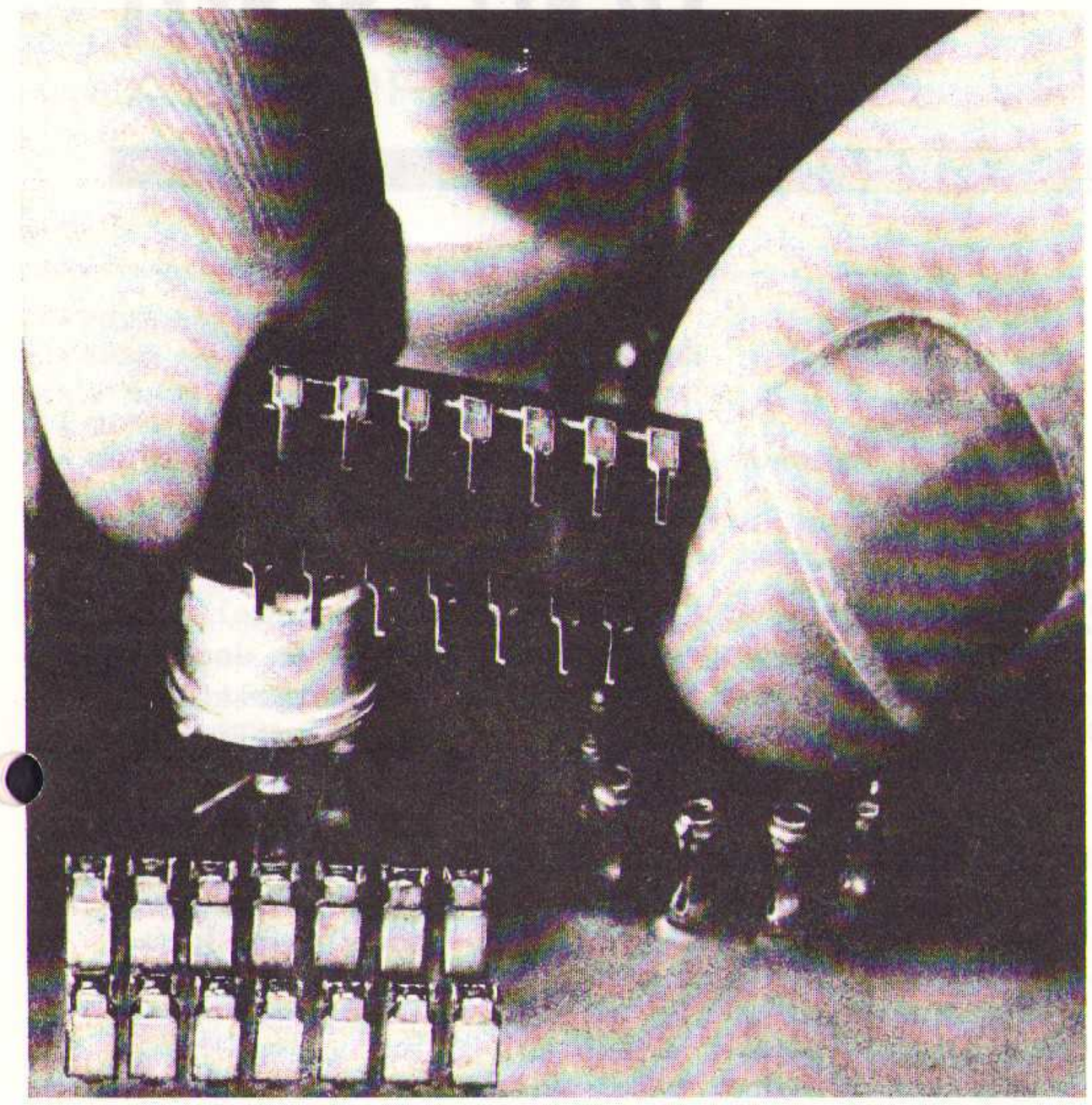
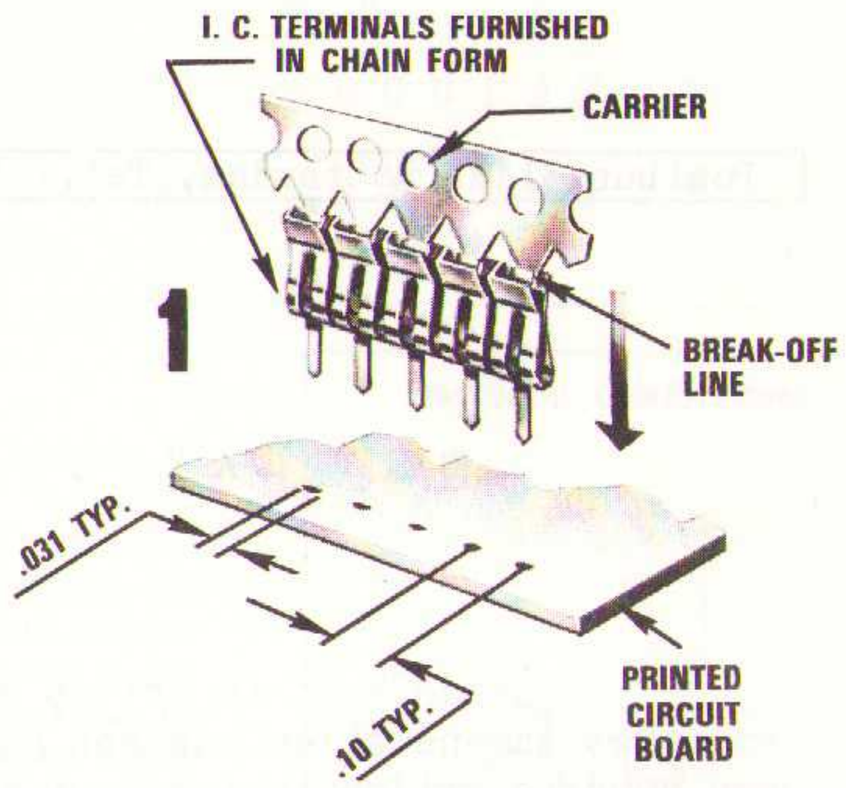
soldercon® terminals 1938-4

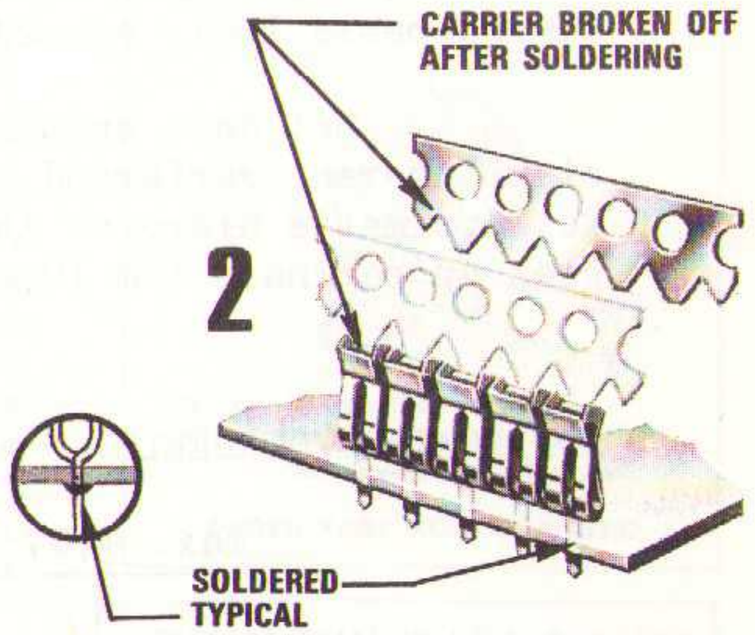
(zelfbouw IC voeten)

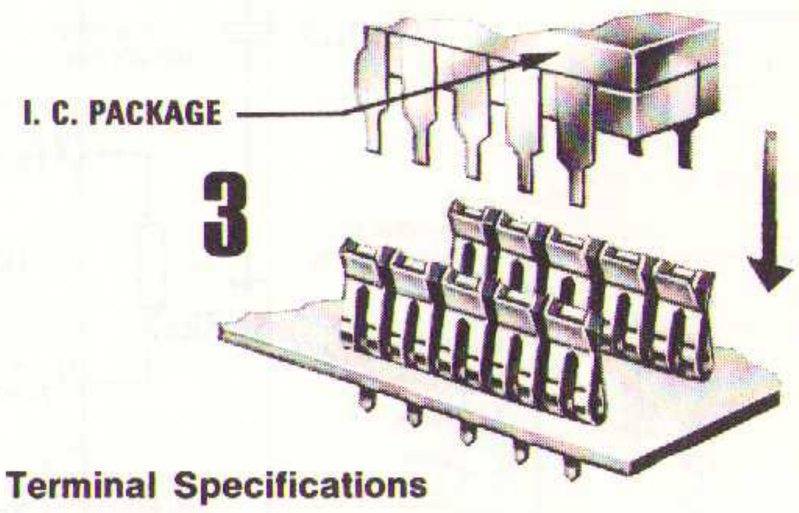


1938-4 Soldercon terminals advance the state-of-the-art by providing manufacturers with the advantages of plug-in packages for connecting integrated circuits at affordable prices.

1938-4 Soldercons are available in chain form . . . or precut in strips to fit your exact I. C. requirements. These terminals provide excellent electrical contact and sturdy mechanical support. Their use speeds assembly, testing and servicing, and gives new flexibility to your entire P.C. assembly. Molex Soldercons are available in tin-plated brass







Terminal Specifications

1. Height above board—.180
2. Hole required
   A. Drilled—.032/.030 diameter
   B. Punched—.032/.030 diameter with .037 diameter maximum breakout
   C. Plated through—.037/.029 diameter
3. Minimum spacing—.100 on centers per row; .200 row spacing
4. Insertion—1 oz min. per terminal
5. Withdraw—¾ oz min. per terminal
6. Lead size range—.007"/.011"x.018"/.030"

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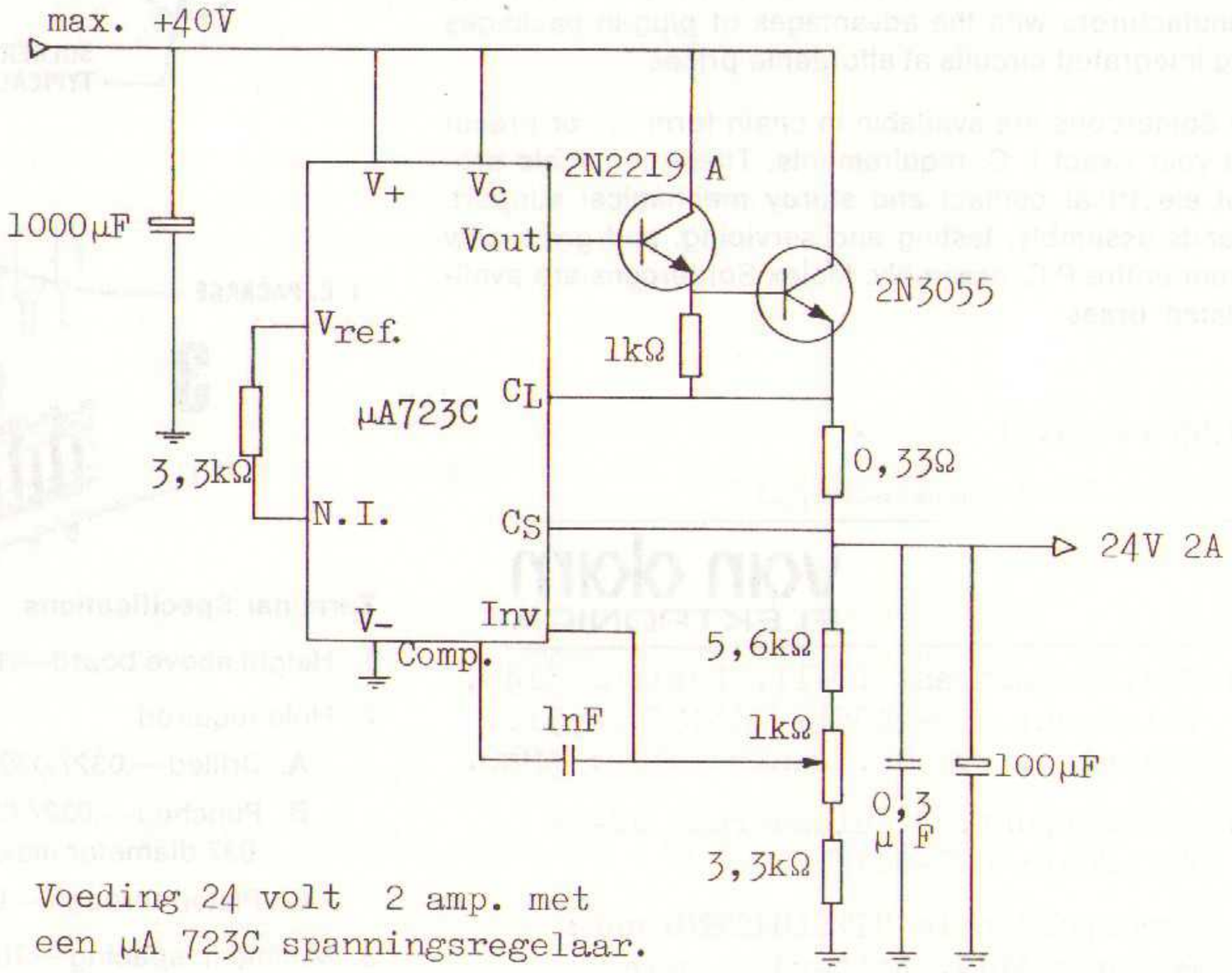
D E µA723C S P A N N I N G S R E G E L A A R

Sinds kort is het op grote schaal toepassen van een spanningsregelaar voor het samenstellen van een goede voeding nog meer verantwoord geworden door een scherpe prijsnotering voor de µA723C van Fairchild. Deze spanningsregelaar kost heden ten dage slechts ƒ 9,90 incl. 12% BTW, waardoor onderstaand applicatievoorbeeld incl. een 2Amp bruggelijkrichter nog slechts ƒ 37,- kost.

Met deze spanningsregelaar is het mogelijk vele voedingsspanningen te stabiliseren, variërend van 3 tot 250 volt (positief of negatief). Een uitgebreide informatie hierover is opgenomen in de vorm van het volledige datasheet, hetgeen op pagina 5 t/m 10 gepubliceerd is.

APPLICATIE-VOORBEELD:



Voeding 24 volt 2 amp. met
een µA 723C spanningsregelaar.

Snellemanstraat 10-11, Rotterdam-noord, Postgiro: 295550. Bankrelatie: AMRO-bank.
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μA723C PRECISION VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

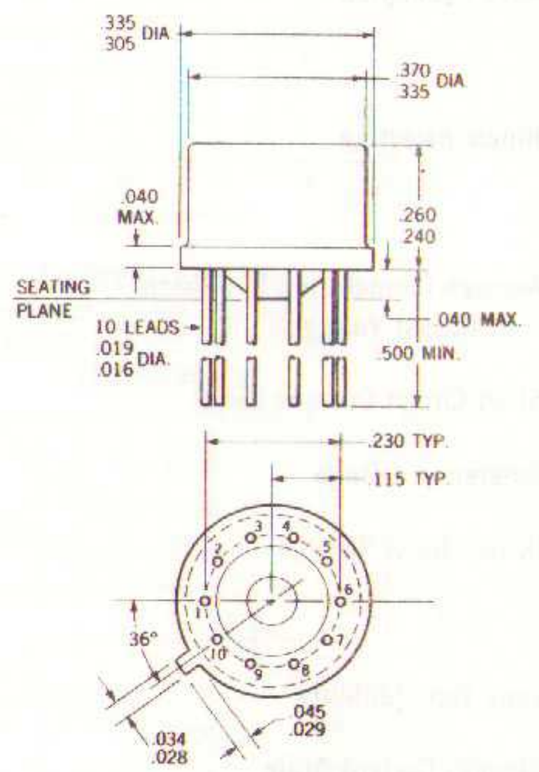
- **POSITIVE OR NEGATIVE SUPPLY OPERATION**
- **SERIES, SHUNT, SWITCHING OR FLOATING OPERATION**
- **.01% LINE AND LOAD REGULATION**
- **OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS**
- **OUTPUT CURRENT TO 150 mA WITHOUT EXTERNAL PASS TRANSISTOR**

GENERAL DESCRIPTION — The μA723C is a monolithic voltage regulator constructed on a single silicon chip using the Fairchild Planar* epitaxial process. The device consists of a temperature compensated reference amplifier, error amplifier, power series pass transistor and current limit circuitry. Additional NPN or PNP pass elements may be used when output currents exceeding 150 mA are required. Provisions are made for adjustable current limiting and remote shutdown. In addition to the above, the device features low standby current drain, low temperature drift and high ripple rejection. The μA723C is intended for use with positive or negative supplies as a series, shunt, switching or floating regulator. Applications include laboratory power supplies, isolation regulators for low level data amplifiers, logic card regulators, small instrument power supplies, airborne systems and other power supplies for digital and linear circuits. For full temperature range operation (−55°C to +125°C), see μA723 data sheet.

ABSOLUTE MAXIMUM RATINGS

Voltage from V^+ to V^-	40 V
Input-Output Voltage Differential	40 V
Maximum Output Current	150 mA
Current from V_Z	25 mA
Current from V_{REF}	15 mA
Internal Power Dissipation—Metal Can (Note 1)	800 mW
Internal Power Dissipation—DIP (Note 1)	900 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

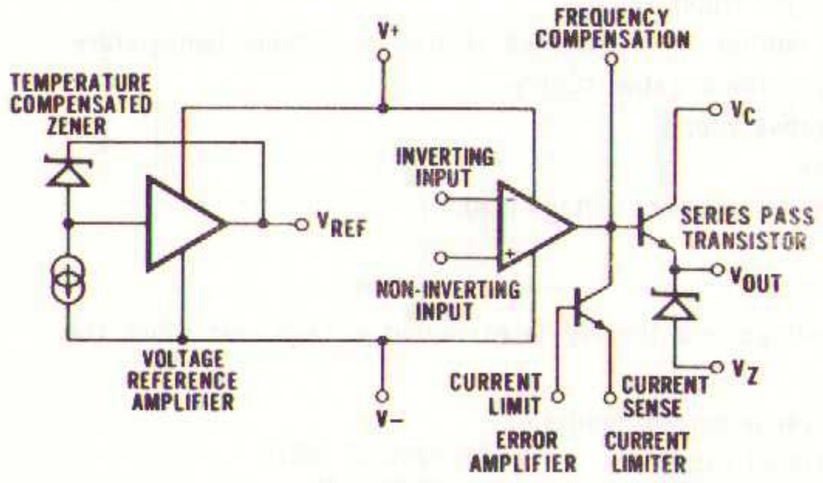
PHYSICAL DIMENSIONS



NOTES: All dimensions in inches
Leads are gold-plated Kovar
Package weight is 1.32 grams

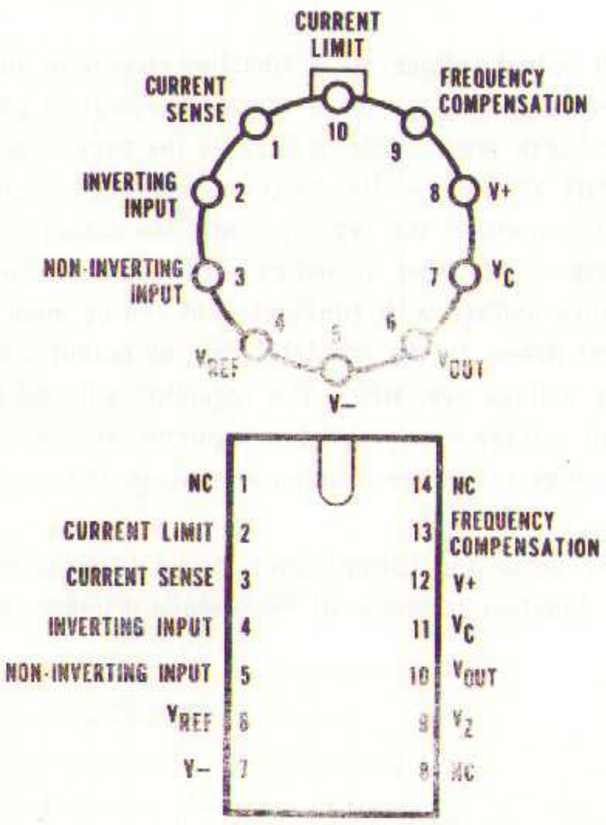
ORDER PART NO. U5R7723393

EQUIVALENT CIRCUIT



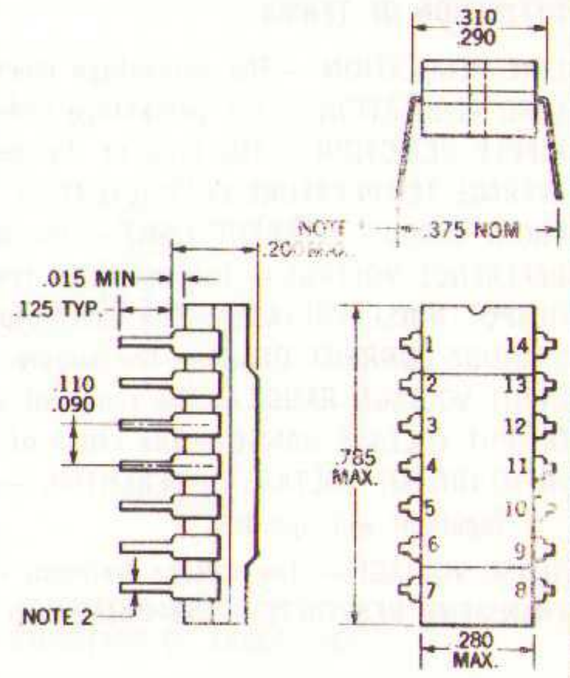
CONNECTION DIAGRAMS

TOP VIEWS



Note: On metal can, pin 5 is connected to case

TYPICAL DUAL IN-LINE PACKAGE



NOTES: All dimensions in inches
Leads are intended for insertion in hole rows, .300 centers

ORDER PART NO. U6A7723393

Notes on Page 6.

*Planar is a patented Fairchild process.

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ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Line Regulation	$V_{IN} = 12\ V$ to $V_{IN} = 15\ V$		.01	0.1	% V_{OUT}
	$V_{IN} = 12\ V$ to $V_{IN} = 40\ V$		0.1	0.5	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $V_{IN} = 12\ V$ to $V_{IN} = 15\ V$			0.3	% V_{OUT}
Load Regulation	$I_L = 1\ mA$ to $I_L = 50\ mA$		.03	0.2	% V_{OUT}
	$0°C \leq T_A \leq 70°C$, $I_L = 1\ mA$ to $I_L = 50\ mA$			0.6	% V_{OUT}
Ripple Rejection	$f = 50\ Hz$ to $10\ kHz$, $C_{REF} = 0$		74		dB
	$f = 50\ Hz$ to $10\ kHz$, $C_{REF} = 5\ \mu F$		86		dB
Average Temperature Coefficient of Output Voltage	$0°C \leq T_A \leq 70°C$		.003	.015	%/°C
Short Circuit Current Limit	$R_{SC} = 10\ \Omega$, $V_{OUT} = 0$		65		mA
Reference Voltage		6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, $C_{REF} = 0$		20		μV_{rms}
	BW = 100 Hz to 10 kHz, $C_{REF} = 5\ \mu F$		2.5		μV_{rms}
Long Term Stability			0.1		%/1000 hrs
Standby Current Drain	$I_L = 0$, $V_{IN} = 30\ V$		2.3	4.0	mA
Input Voltage Range		9.5		40	V
Output Voltage Range		2.0		37	V
Input-Output Voltage Differential		3.0		38	V

DEFINITION OF TERMS

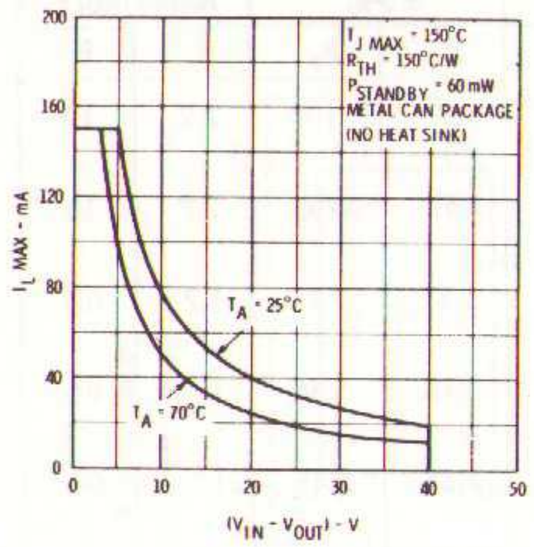
LINE REGULATION — The percentage change in output voltage for a specified change in input voltage.
LOAD REGULATION — The percentage change in output voltage for a specified change in load current.
RIPPLE REJECTION — The ratio of the peak to peak input ripple voltage to the peak to peak output ripple voltage.
AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE — The percentage change in output voltage for a specified change in ambient temperature.
SHORT CIRCUIT CURRENT LIMIT — The output current of the regulator with the output shorted to the negative supply.
REFERENCE VOLTAGE — The output of the reference amplifier measured with respect to the negative supply.
OUTPUT NOISE VOLTAGE — The rms output noise voltage with constant load and no input ripple.
STANDBY CURRENT DRAIN — The supply current drawn by the regulator with no output load and no reference voltage load.
INPUT VOLTAGE RANGE — The range of supply voltage over which the regulator will operate.
OUTPUT VOLTAGE RANGE — The range of output voltage over which the regulator will operate.
INPUT-OUTPUT VOLTAGE DIFFERENTIAL — The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.
SENSE VOLTAGE — The voltage between current sense and current limit terminals necessary to cause current limiting.
TRANSIENT RESPONSE — The closed-loop step function response of the regulator under small-signal conditions.

NOTES:

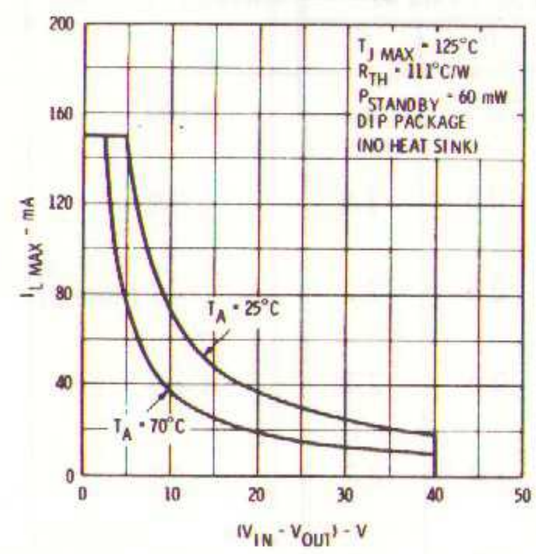
(1) Derate metal can package at 6.8 mW/°C and dual in-line package at 9 mW/°C for operation at ambient temperatures above 25°C.
(2) Unless otherwise specified, $T_A = 25°C$, $V_{IN} = V^+ = V_C = 12\ V$, $V^- = 0$, $V_{out} = 5\ V$, $I_L = 1\ mA$, $R_{SC} = 0$, $C_1 = 100\ pF$, $C_{REF} = 0$, divider impedance as seen by error amplifier $\leq 10\ k\Omega$, and connected as shown in Figure 1.
(3) For metal can applications where V_Z is required, an external 6.2 zener should be connected in series with V_{out}.
(4) Figures in parentheses may be used if R_1/R_2 divider is placed on opposite side of error amp.
(5) Replace R_1/R_2 in figures with divider shown in figure 13.
(6) V^+ must be connected to a +3 V or greater supply.
(7) L_1 is 40 turns of #20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009" air gap.

TYPICAL PERFORMANCE CURVES

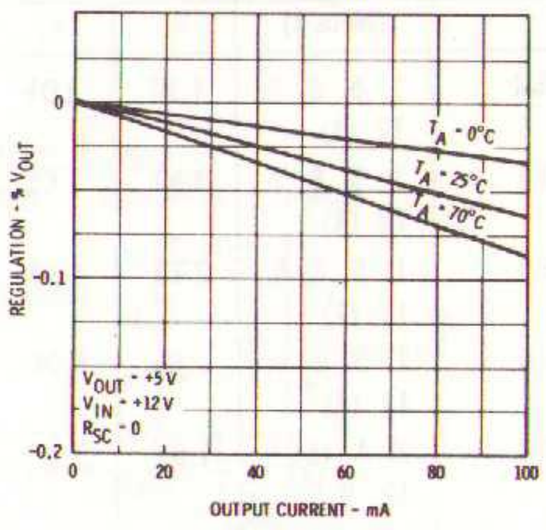
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



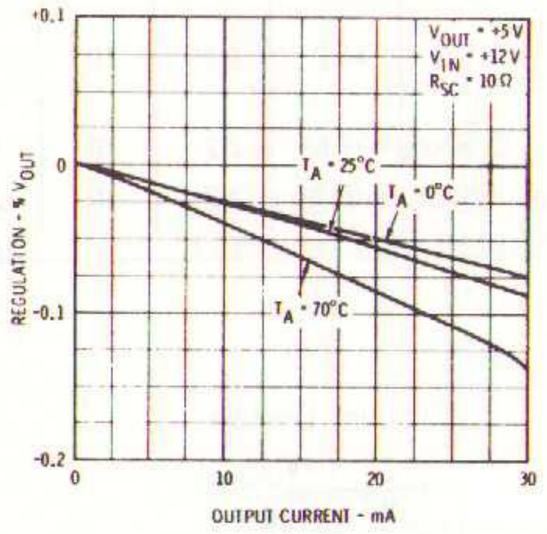
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



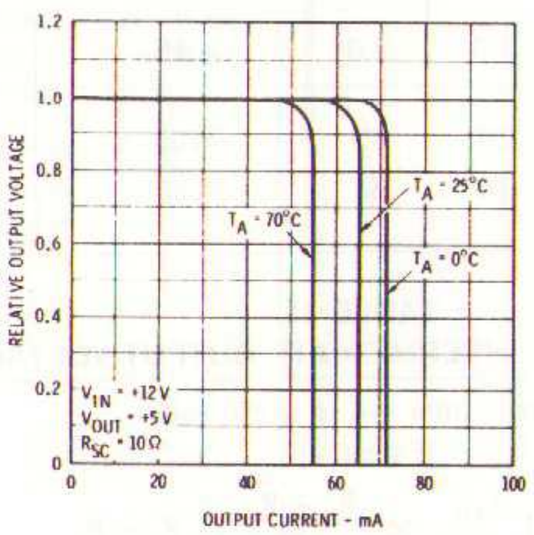
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



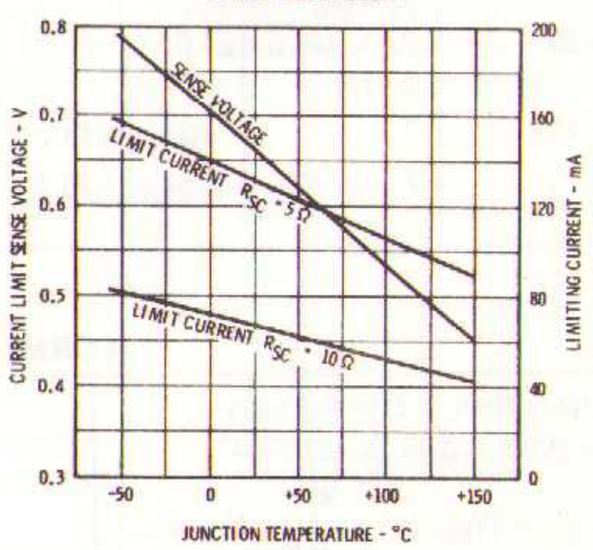
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



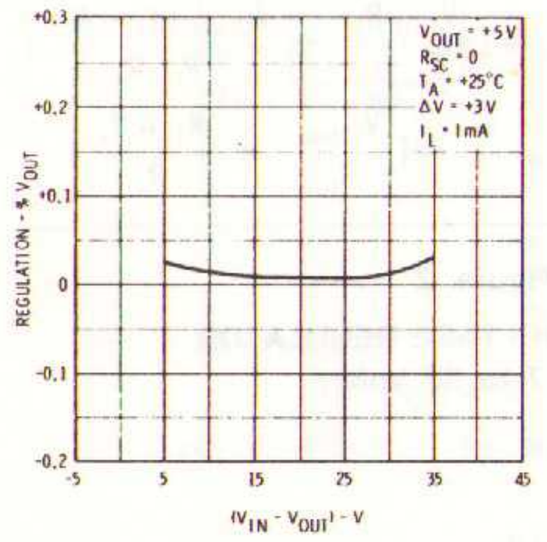
CURRENT LIMITING CHARACTERISTICS



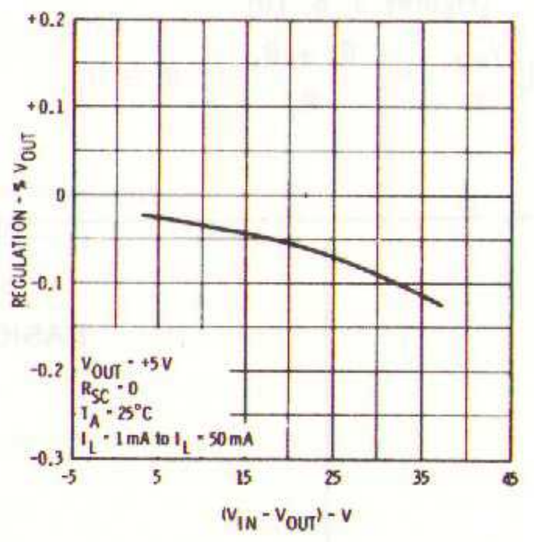
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPERATURE



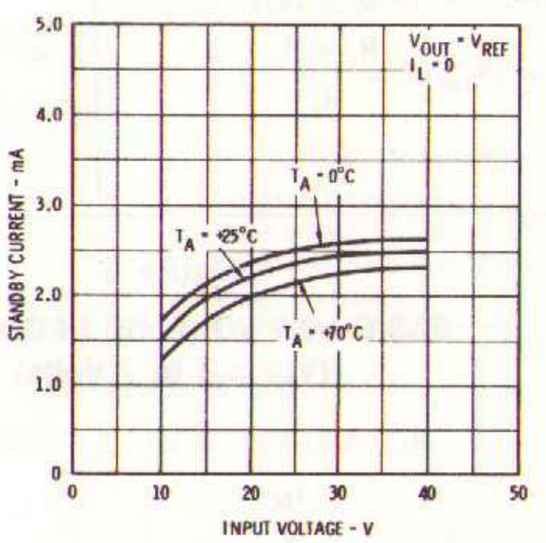
LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



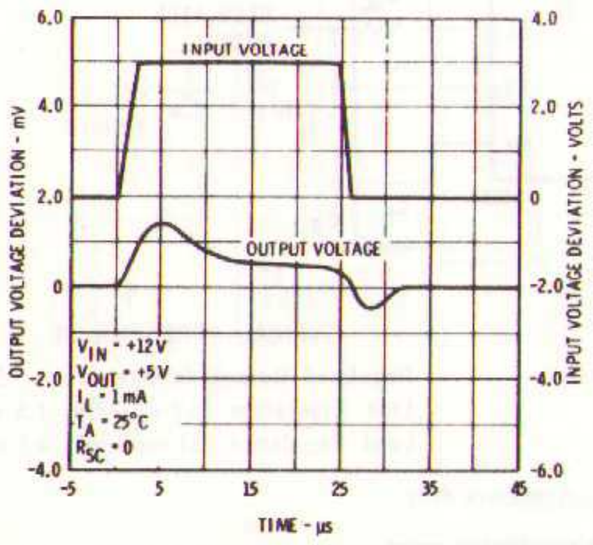
LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



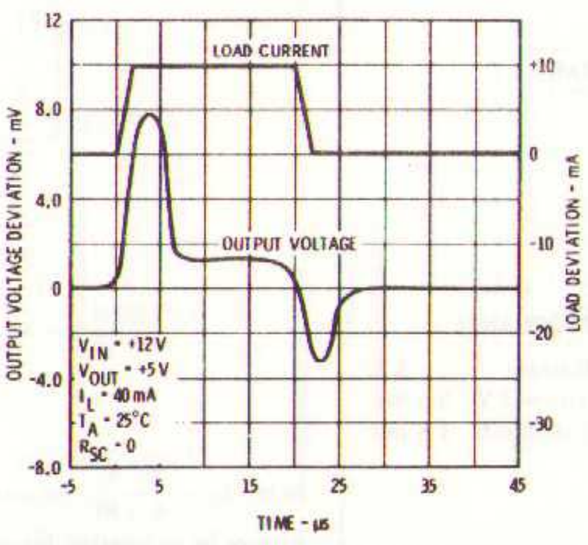
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

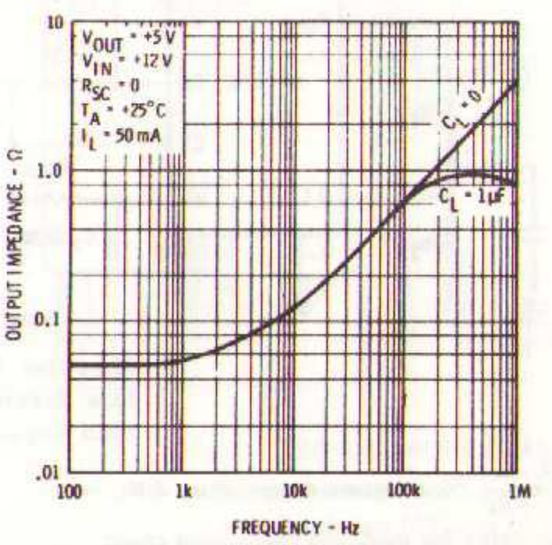


TABLE I
RESISTOR VALUES (kΩ) FOR STANDARD OUTPUT VOLTAGES

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R_1	R_2	R_1	P_1	R_2			R_1	R_2	R_1	P_1	R_2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II
FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts
[Figures 1, 5, 6, 9, 12, (4)]

$$V_{OUT} = [V_{REF} \times \frac{R_2}{R_1 + R_2}]$$

Outputs from +4 to +250 volts
[Figure 7]

$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_2 - R_1}{R_1}]\ ;\ R_3 = R_4$$

Current Limiting

$$I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$$

Outputs from +7 to +37 volts
[Figures 2, 4, (5, 6, 9, 12)]

$$V_{OUT} = [V_{REF} \times \frac{R_1 + R_2}{R_2}]$$

Outputs from −6 to −250 volts
[Figures 3, 8, 10]

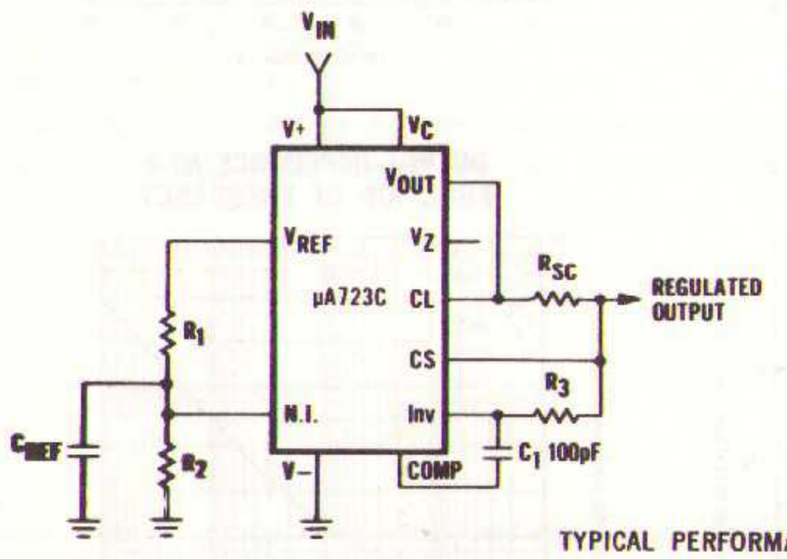
$$V_{OUT} = [\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}]\ ;\ R_3 = R_4$$

Foldback Current Limiting

$$I_{KNEE} = [\frac{V_{OUT}\, R_3}{R_{SC}\, R_4} + \frac{V_{SENSE}\,(R_3 + R_4)}{R_{SC}\, R_4}]$$

$$I_{SHORT\ CKT} = [\frac{V_{SENSE}}{R_{SC}} \times \frac{R_3 + R_4}{R_4}]$$

Figure 1
BASIC LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

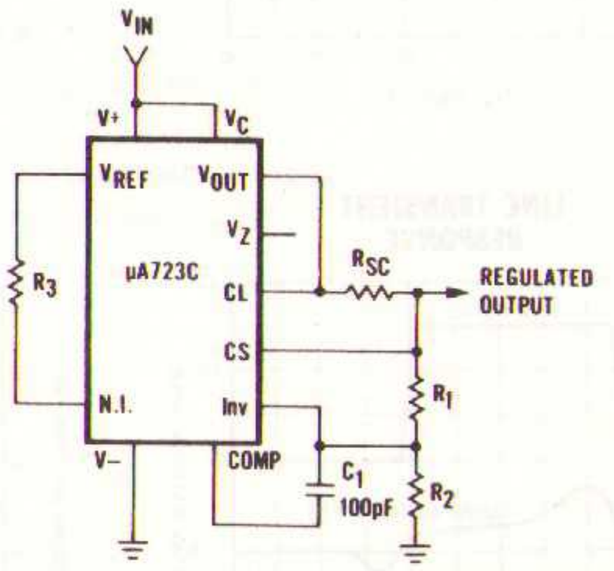


TYPICAL PERFORMANCE

Regulated Output Voltage	5 V
Line Regulation (ΔV_{IN} = 3 V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 2
BASIC HIGH VOLTAGE REGULATOR
(V_{out} = 7 to 37 Volts)

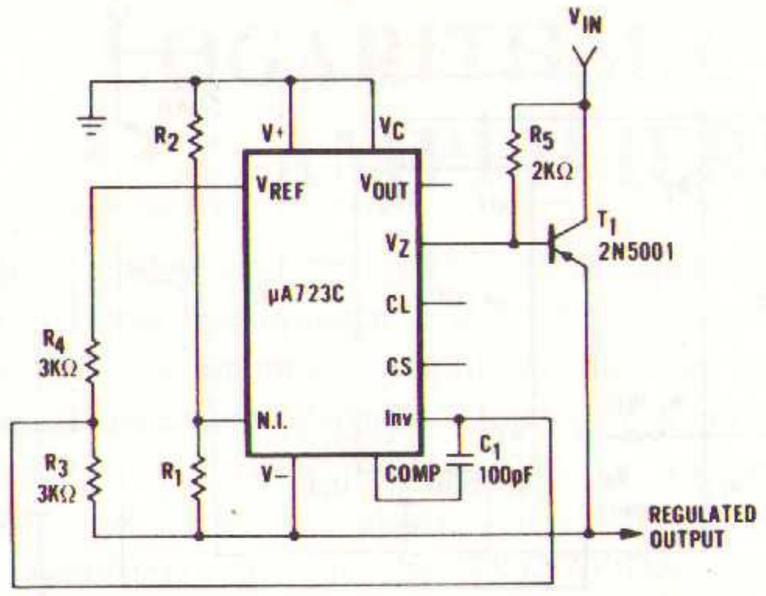


TYPICAL PERFORMANCE

Regulated Output Voltage	15 V
Line Regulation (ΔV_{IN} = 3 V)	1.5 mV
Load Regulation (ΔI_L=50 mA)	4.5 mV

Note: $R_3 = \frac{R_1\ R_2}{R_1 + R_2}$ for minimum temperature drift.
R_3 may be eliminated for minimum component count.

Figure 3
NEGATIVE VOLTAGE REGULATOR

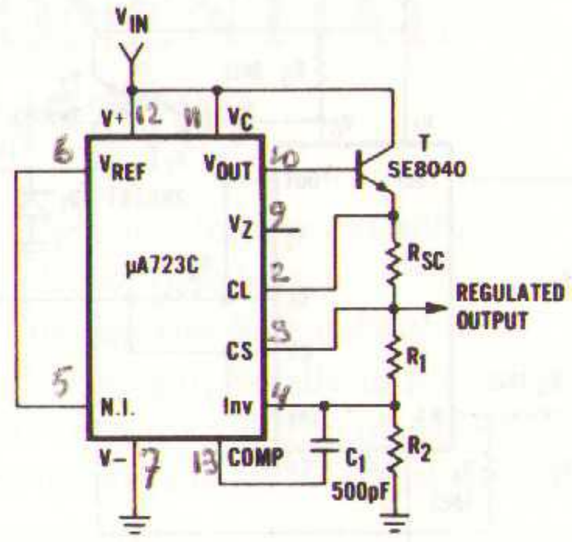


TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1 mV
Load Regulation ($\Delta I_L = 100$ mA)	2 mV

Note 3

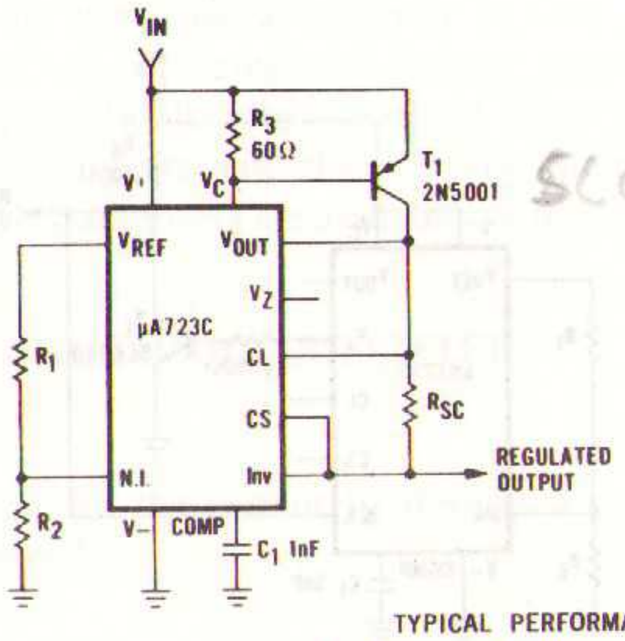
Figure 4
POSITIVE VOLTAGE REGULATOR
(External NPN Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+15 V
Line Regulation ($\Delta V_{IN} = 3$ V)	1.5 mV
Load Regulation ($\Delta I_L = 1$ A)	15 mV

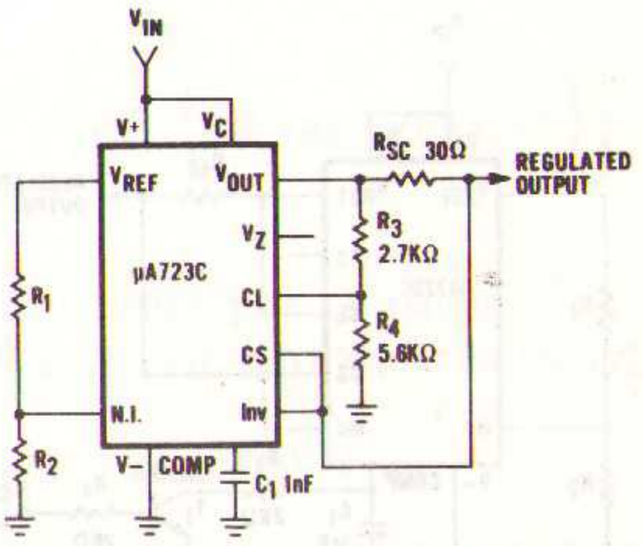
Figure 5
POSITIVE VOLTAGE REGULATOR
(External PNP Pass Transistor)



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 1$ A)	5 mV

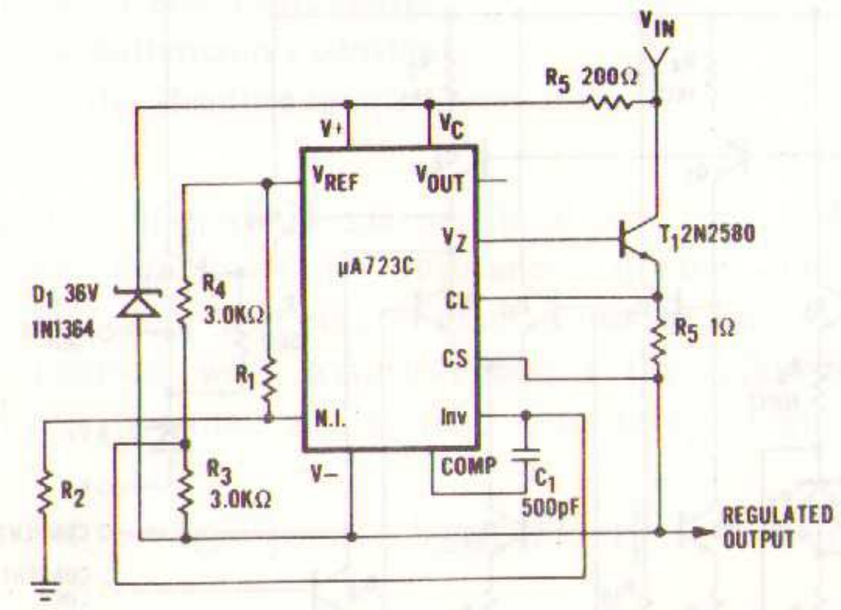
Figure 6
FOLDBACK CURRENT LIMITING



TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation ($\Delta I_L = 10$ mA)	1 mV
Current Limit Knee	20 mA

Figure 7
POSITIVE FLOATING REGULATOR

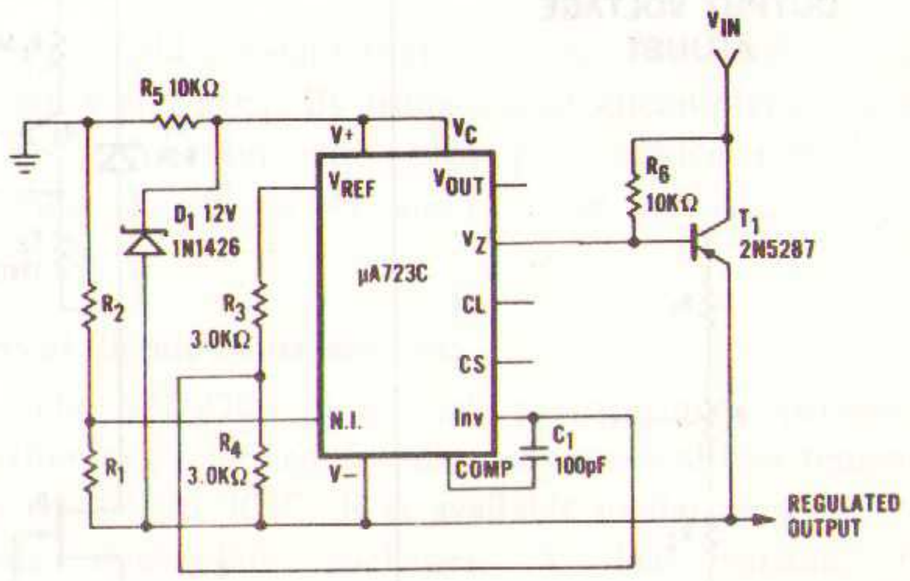


TYPICAL PERFORMANCE

Regulated Output Voltage	+50 V
Line Regulation ($\Delta V_{IN} = 20$ V)	15 mV
Load Regulation ($\Delta I_L = 50$ mA)	20 mV

Note 3

Figure 8
NEGATIVE FLOATING REGULATOR



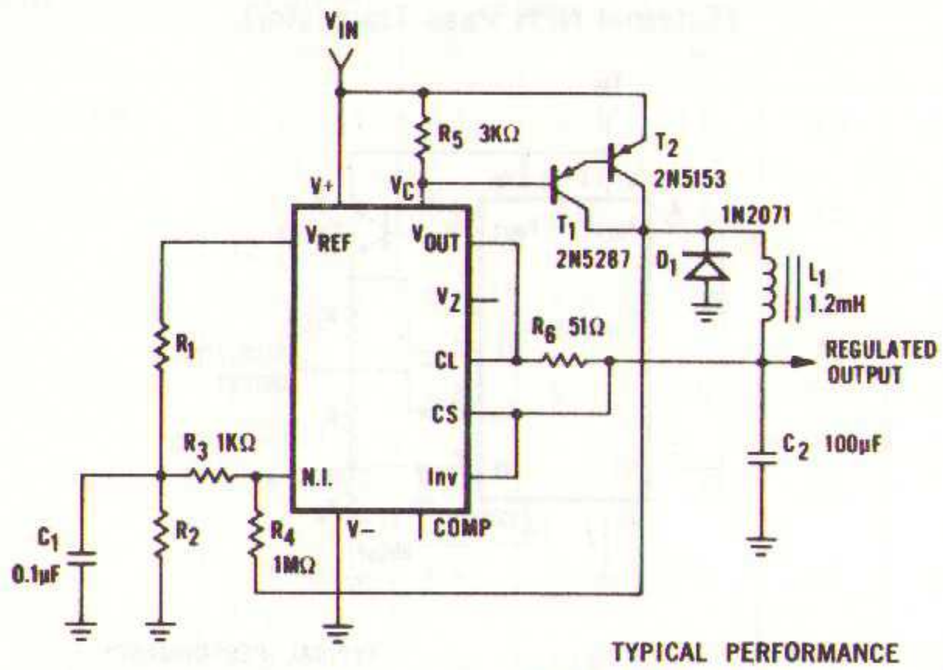
TYPICAL PERFORMANCE

Regulated Output Voltage	−100 V
Line Regulation ($\Delta V_{IN} = 20$ V)	30 mV
Load Regulation (ΔI_L=100 mA)	20 mV

Note 3

Figure 9

POSITIVE SWITCHING REGULATOR



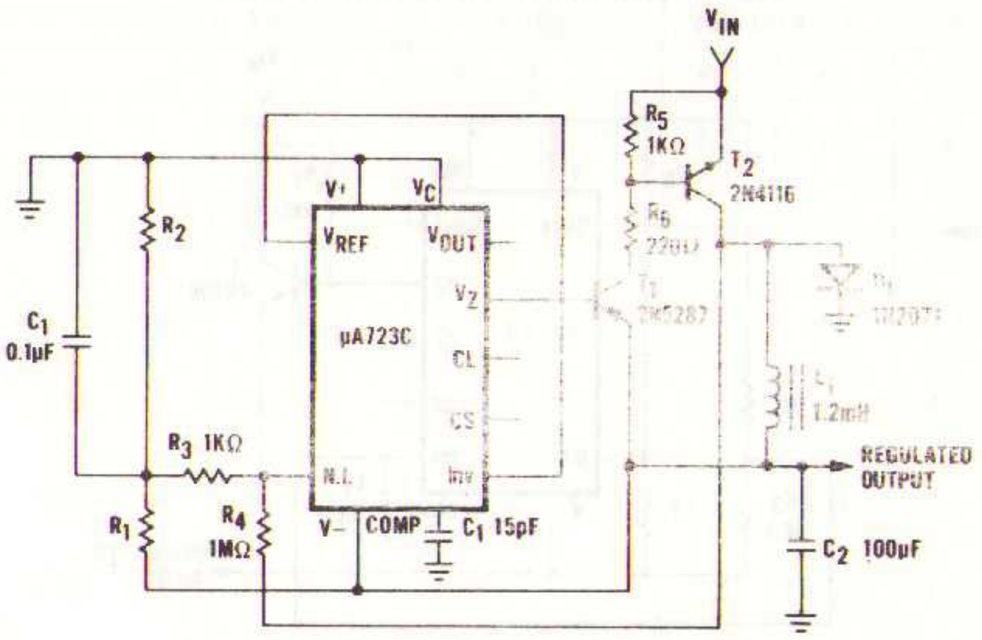
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 30$ V)	10 mV
Load Regulation ($\Delta I_L = 2$ A)	80 mV

Note 7

Figure 10

NEGATIVE SWITCHING REGULATOR



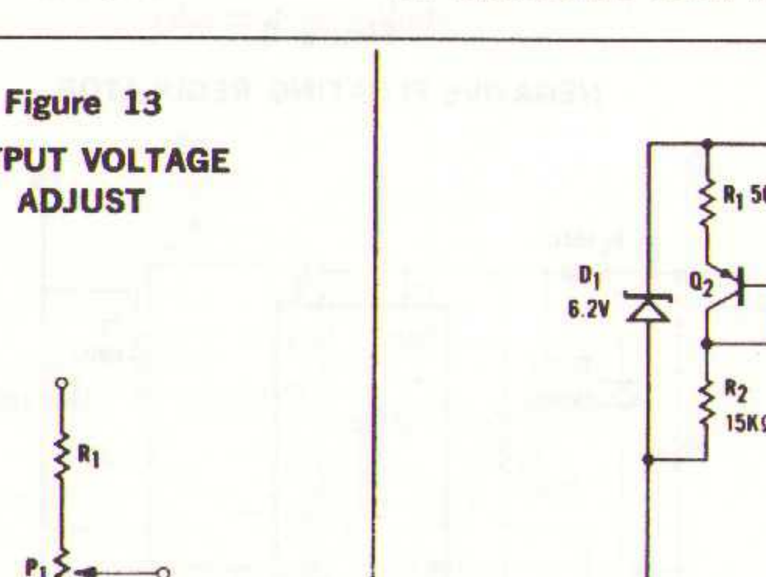
TYPICAL PERFORMANCE

Regulated Output Voltage	−15 V
Line Regulation ($\Delta V_{IN} = 20$ V)	8 mV
Load Regulation ($\Delta I_L = 2$ A)	6 mV

Note 3
Note 7

Figure 11

REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



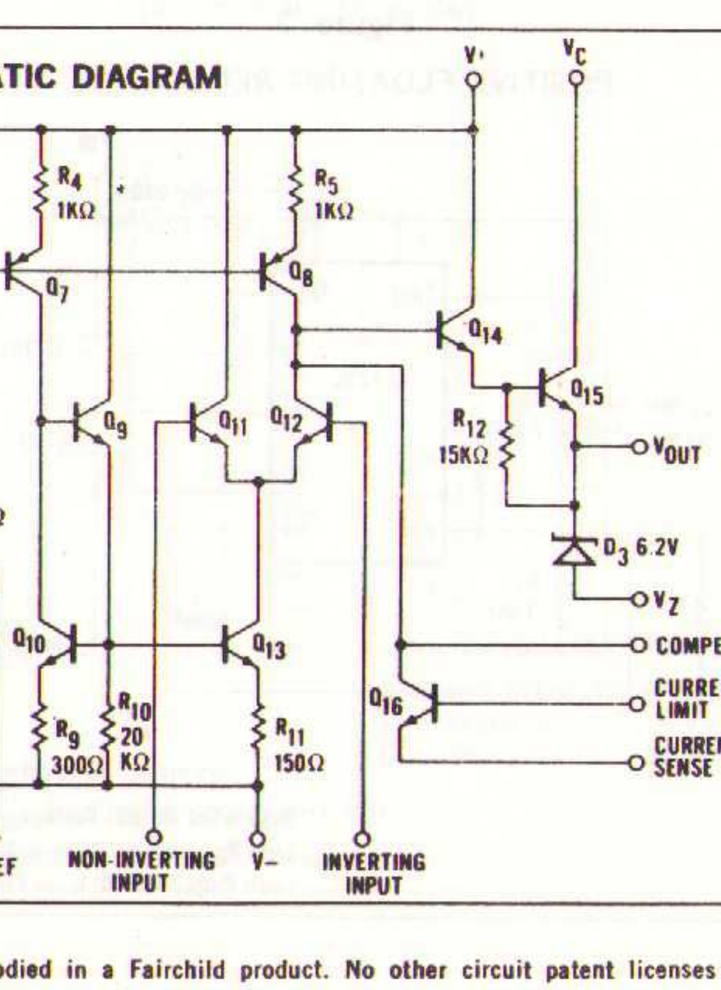
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 3$ V)	0.5 mV
Load Regulation (ΔI_L=50 mA)	1.5 mV

Note: Current limit transistor may be used for shutdown if current limiting is not required.

Figure 12

SHUNT REGULATOR



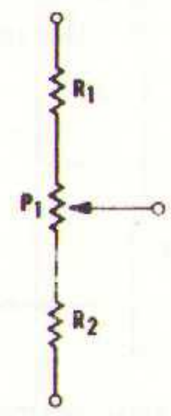
TYPICAL PERFORMANCE

Regulated Output Voltage	+5 V
Line Regulation ($\Delta V_{IN} = 10$ V)	0.5 mV
Load Regulation ($\Delta I_L = 100$ mA)	1.5 mV

Note 3

Figure 13

OUTPUT VOLTAGE ADJUST



SCHEMATIC DIAGRAM

LOGARITHMIC AND EXPONENTIAL AMPLIFIERS WITH SN72709

Using simple circuitry and the SN72709DN operational amplifier from Texas Instruments, it is possible to produce logarithmic and exponential amplifiers having good linearity over at least three decades. These amplifiers may be connected together to form power-law or multiplier systems. The low cost of plastic encapsulated dual operational amplifiers such as the SN72709DN, makes these systems particularly attractive. The fact that the systems can be made almost independent of ambient temperature gives them a considerable advantage when compared with diode function generators and other forms of non-linear circuit.

respectively. Both circuits rely on the exponential relationship between a transistor's collector current and its base-emitter voltage. In each case a transistor is used as the feedback element of an integrated circuit operational amplifier. The report also describes a method for producing an amplifier having a power-law characteristic for powers between 4 and 1/4. Data sheets are available on request.

LOGARITHMIC AMPLIFIER

Theory

The basic equation for the current I_D through a semiconductor diode is given by:

$$I_D = I_S \cdot \left\{\exp (qV/k\bar{T}) - 1\right\}$$

where I_S is the saturation current of the diode
V is the forward voltage across the diode
q is the electronic charge
k is Boltzmann's constant
and T is the absolute temperature

In practice this relationship does not hold over a very wide range largely due to finite resistances in the diode. However, by using the emitter-base diode action of a transistor coupled with transistor action the following relationship is obtained and is valid over seven or more decades:

$$I_{CS} = I_O \left\{\exp (q\, V_{EB}/kT) - 1\right\} \qquad (1)$$

where I_{CS} is the collector current with zero collector-base bias
V_{EB} is the emitter-base voltage
and I_O is a constant, usually in the region of 10^{-15}A for a silicon planar transistor. It is constant for all transistors of a given type.

For $I_{CS} \geqslant 1$nA, Equation (1) may be modified to

$$I_{CS} = I_O \cdot \left\{\exp (qV_{EB}/kT)\right\} \qquad (2)$$

For two transistors having collector currents I_{CS1} and I_{CS2} the ratio of these currents is given by

$$\frac{I_{CS1}}{I_{CS2}} = \left[\exp \left\{q(V_{EB1} - V_{EB2})/kT\right\}\right] \cdot \frac{I_{O1}}{I_{O2}} \qquad (3)$$

For a closely matched pair of transistors as in a dual transistor, $V_{EB1} \cong V_{EB2}$, I_{O1} approximates I_{O2}

and $$I_{CS1}/I_{CS2} = \exp (qV/kT) \qquad (4)$$

where for a temperature of 25°C, kT/q = 25.7 mV.
From Equation (4) it is apparent that if I_{CS2} is held constant, there is an exponential relationship between I_{CS1} and V. Taking natural logarithms of both sides of Equation (4)

$$V = \frac{kT}{q} \cdot \log_\epsilon \left[I_{CS1}/I_{CS2}\right] \qquad (5)$$

If I_{CS2} is held constant there is a logarithmic relationship between V and I_{CS1}. By using a dual silicon-planar transistor in conjunction with high performance operational amplifiers Equations (4) and (5) can be realized very accurately.

Practical Circuit Considerations

The SN72709 is a high performance operational amplifier characterized for use between ambient temperatures of 0°C to 70°C. It is available in flat pack, TO5 or plastic dual-in-line packages. A dual version, the SN72709DN, is available in plastic DIL package only. This package contains two separate amplifier chips which are electrically isolated from their $V_{CC}+$ and $V_{CC}-$ supplies. Since the two amplifiers are not on the same substrate there

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This report is adapted from the original "Simple Logarithmic and Exponential Amplifiers" by Denis Spicer and Richard Mann, published by Texas Instruments Ltd., Bedford, England.

is no possibility of thermal coupling as in monolithic dual amplifiers. The pin connections for the SN72709DN are shown in Figure 1 and its main characteristics are shown in Table I. For applications requiring a tighter specification or operation over a wider temperature range the SN52709 should be used. These amplifiers are suitable for operation in the temperature range −55°C to 125°C and can be obtained in various versions with different spreads in electrical characteristics.

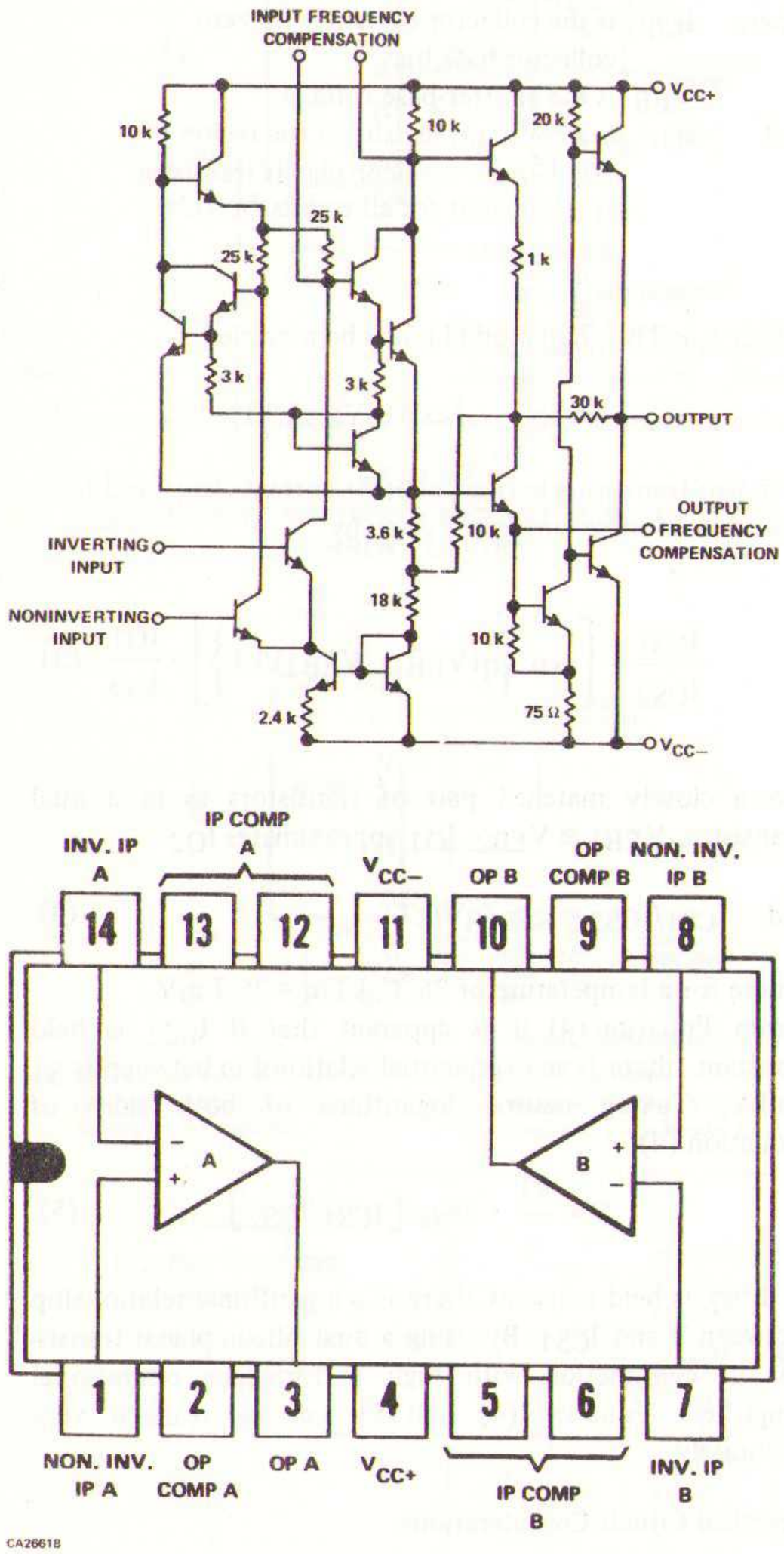

FIGURE 1. Schematic and Package Configuration of the SN72709DN

The circuit of the logarithmic amplifier is shown in Figure 2. Operational amplifiers OA1 and OA2 are the two halves of a SN72709DN. The first half OA1 is used to define the collector current ICS1 of transistor Q1. When OA1 is connected as shown in Figure 2, making the usual assumptions of infinite gain and negligible input current for the amplifier, we obtain

$$I_{CS1} = V_{in}/R4 \tag{6}$$

The second amplifier OA2, is used in non-inverting configuration to provide a high input impedance at the base of transistor Q2 and to give a voltage gain of 30. The collector current ICS2 of transistor Q2, is defined by the stable reference voltage V_{ref} and by resistor R3. It is assumed that the base voltage of Q2 which is between −30 mV and +400 mV is negligible compared with the V_{ref} and therefore

$$I_{CS2} = V_{ref}/R3 \tag{7}$$

Since I_{CS1} and I_{CS2} are now defined it is possible to evaluate V according to Equation (5). As the base of Q1 is grounded, V is also the input to OA2. The expression for V_{out} is:

$$V_o = \frac{kT}{q} \cdot \frac{(R1+R2)}{R2} \log_e \frac{V_{in}}{R4} \cdot \frac{R3}{V_{ref}} \tag{8}$$

In order to set the zero crossing point in the logarithmic amplifier a d-c offset control R6 is added to make $V_o = 0$ for $V_{in} = 5$ V. This value of crossing point was chosen to enable the logarithmic amplifier to work with the exponential amplifier described later. Therefore, for the circuit values given in Figure 2 and an ambient temperature of 25°C

$$V_o = -3.552 \log_e V_{in}/5\ V \tag{9}$$

A further control R5, is used to compensate for the differential-input offset voltage V_{D10} of amplifier OA1. The adjustment procedure is as follows:

V_{in} is set to 0, the voltage at pin 3 of OA1 is measured, and R5 adjusted until this voltage is less than 50 μV.

V_{in} is set equal to V_{ref} R4/R3 (5 V), the output voltage of OA2 at pin 10 measured, and R6 is adjusted to give zero output voltage.

Performance Characteristics

The d-c transfer characteristic of the logarithmic amplifier is shown in Figure 3. This shows that the amplifier has good linearity over four decades. A major limitation for low values of V_{in} is the maximum output voltage that can be obtained from the operational amplifiers. This output voltage is restricted to a maximum of +14 V under no load conditions and is less than +14 V when a load is applied. When the input current is of the same order as the input bias current of the operational amplifier (about 100 nA) the slope of the transfer characteristic increases as the input decreases.

Table I. Performance Characteristics of the SN72709DN

Electrical characteristics V_{CC+} = 15 V and V_{CC-} = −15 V, (unless otherwise noted, T_A = 25°C)

	PARAMETER	TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage	$R_S \leq 10$ k	T_A = 0°C to 70°C				10	mV
		$R_S \leq 10$ k				2	7.5	mV
I_{DI}	Differential-input offset current	T_A = 0°C to 70°C					750	nA
						100	500	nA
I_{in}	Input current	T_A = 0°C					2	μA
						0.3	1.5	μA
V_{OM}	Maximum peak-to-peak output voltage	$R_L \geq 10$ k			±12	±14		V
		$R_L \geq 2$ k			±10	±13		V
V_{CMI}	Common-mode input voltage range				±8	±10		V
A_V	Large-signal voltage gain	$R_L \geq 2$ k	V_{out} = ±10 V	T_A = 0°C to 70°C	12,000			
		$R_L \geq 2$ k	V_{out} = ±10 V		15,000	45,000		
CMRR	Common-mode rejection ratio	$R_S \leq 10$ k			65	90		dB
SVRR	Supply voltage rejection ratio	$R_S \leq 10$ k				25	200	μV/V
		0°C to 70°C			35			k
r_{in}	Input resistance				50	250		k
r_{out}	Output resistance					150		Ω
P_T	Total power dissipation					80	200	mW

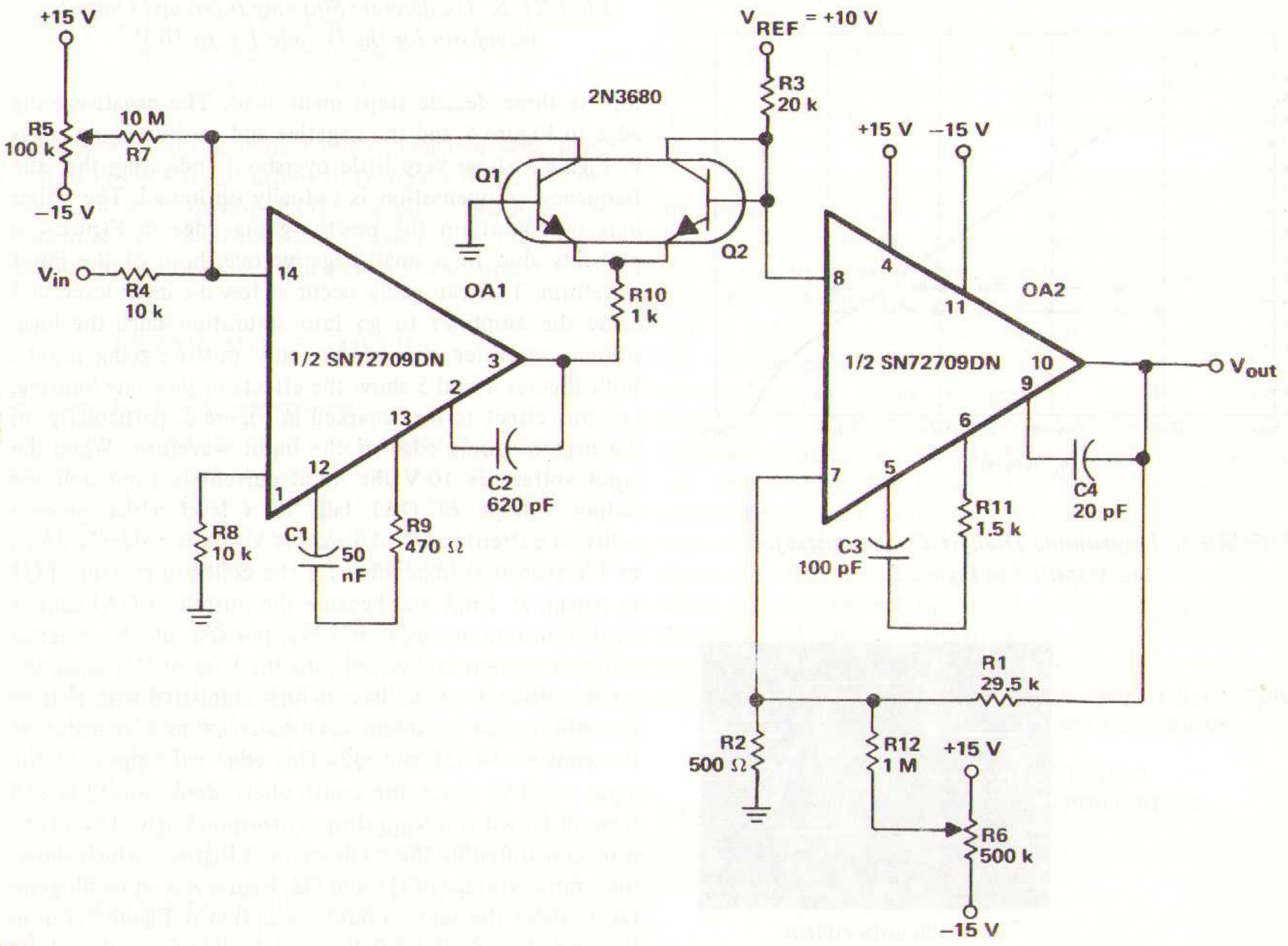

FIGURE 2. Circuit Diagram Showing Two SN72709DNs Connected as a Logarithmic Amplifier

There is a considerable departure from linearity about V_{in} = 20 V where I_{CS1} = 2 mA. Since the transistors used for Q1 and Q2 were small geometry devices, the collector and base bulk resistances become significant at higher values of collector and base current causing a departure from the true logarithmic law.

Because the feedback path around amplifier OA1 is a grounded-base stage there is a considerable voltage gain between the emitter and collector of transistor Q1. Furthermore, the impedance presented to the output of OA1 by the emitter of Q1 will change with frequency. To reduce the effect of these parameters, resistor R10 is added. However, the frequency compensation required on the operational amplifier will still be more than on an amplifier having a non-active feedback element. The high value of the frequency compensation capacitors C1 and C2 limits the frequency response of the amplifier and more significantly, reduces the slew rate of the amplifier. The graph in Figure 3 shows the response times for step inputs covering the decades 10 mV to 100 mV, 100 mV to 1 V and 1 V to 10 V respectively. These times are not true rise and fall times, but give an indication of the approximate settling time of the complete logarithmic amplifier for increasing and decreasing decade inputs. The oscillograms in Figures 4, 5, and 6 show the input and output waveforms

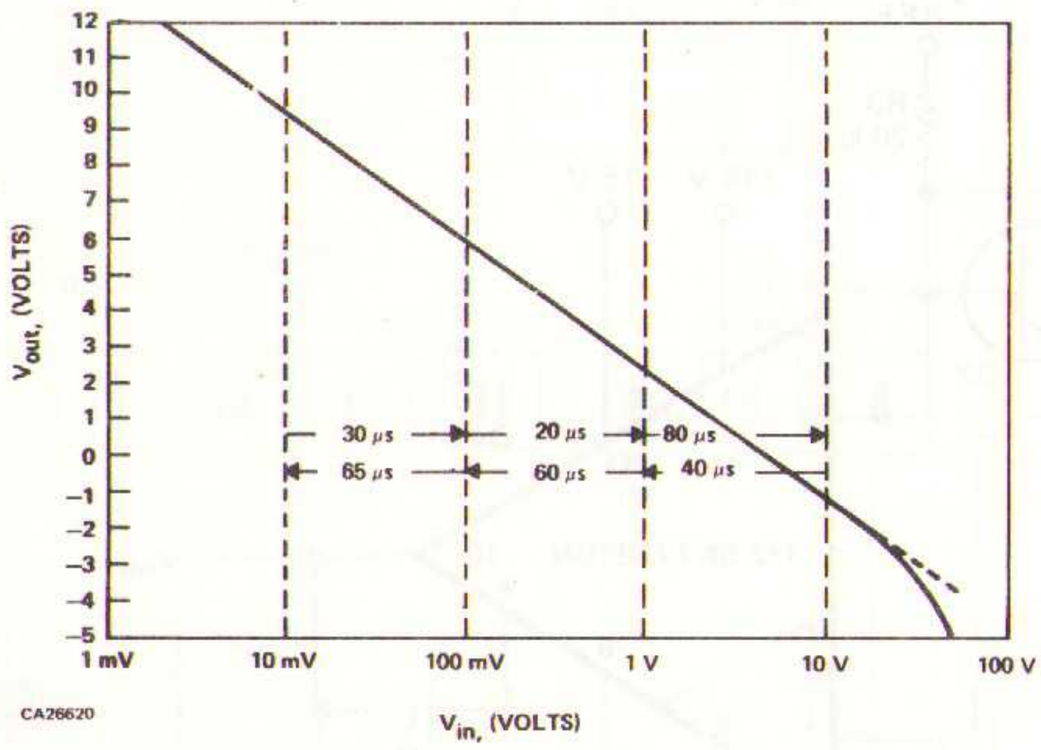

FIGURE 3. Logarithmic Transfer Characteristic for the Amplifier in Figure 2

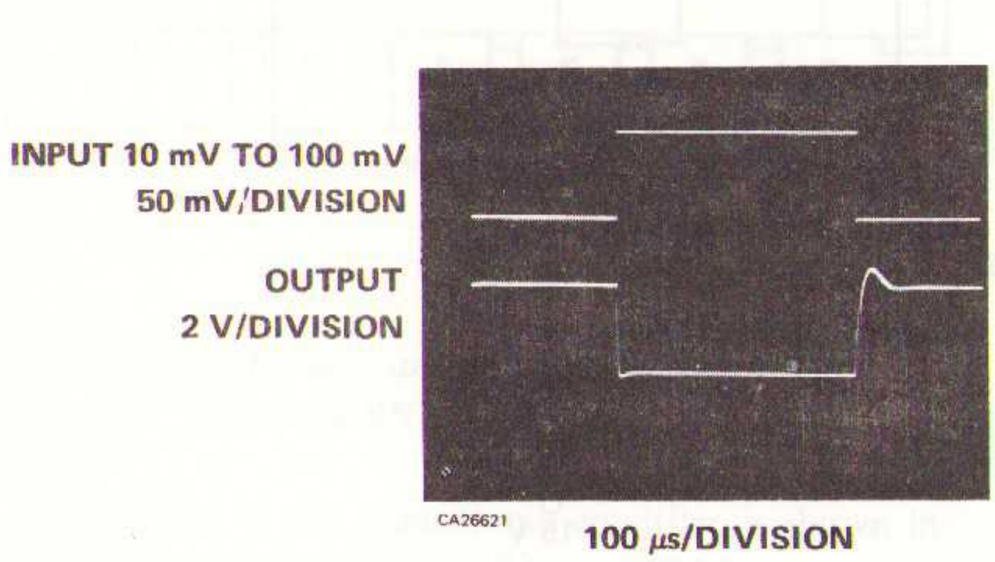

FIGURE 4. Oscillogram Showing Input and Output Waveforms for the Decade 10 mV to 100 mV

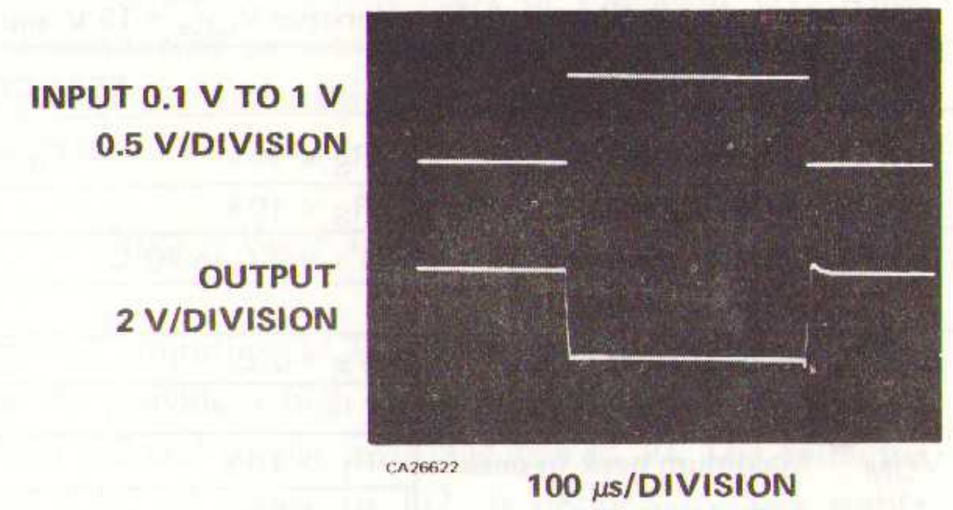

FIGURE 5. Oscillogram Showing Input and Output Waveform for the Decade 100 mV to 1 V

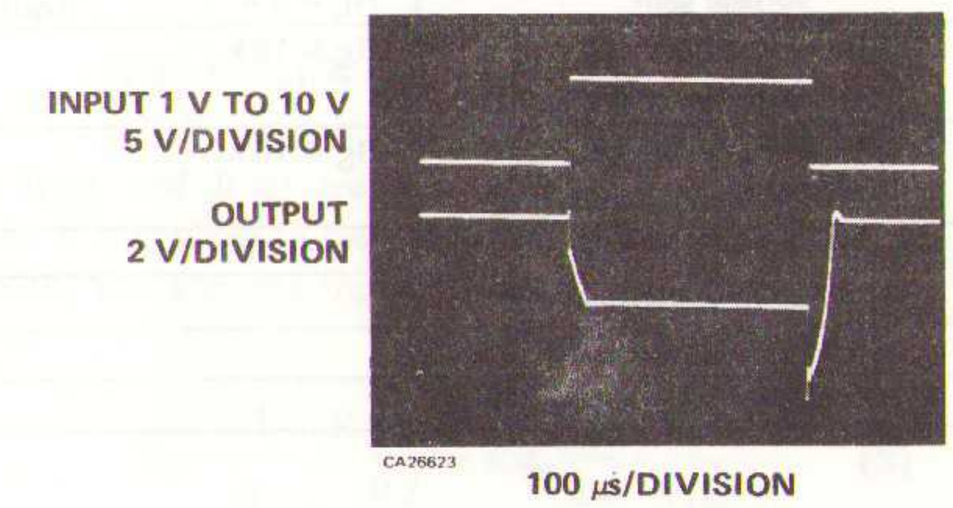

FIGURE 6. Oscillogram Showing Input and Output Waveform for the Decade 1 V to 10 V

for the three decade steps mentioned. The negative-going edge in Figure 4 and the negative and positive-going edges in Figure 5 show very little overshoot indicating that the frequency compensation is virtually optimised. The rather long overshoot on the positive-going edge in Figure 4 is probably due to a small negative overshoot of the input waveform. This can easily occur at low d-c input levels and cause the amplifier to go into saturation since the logarithmic amplifier can handle only positive-going inputs. Both Figures 4 and 5 show the effects of slew rate limiting, but this effect is very marked in Figure 6, particularly on the negative-going edge of the input waveform. When the input voltage is 10 V the input current is 1 mA and the output voltage of OA1 falls to a level which gives a collector current in Q1 of 1 mA. If V_{in} now suddenly drops to 1 V then it is impossible for the collector current of Q1 to remain at 1 mA and because the output of OA1 cannot change instantaneously, a large portion of the original collector current is diverted into the base of Q1. Since the series resistance of the base is high compared with that of the collector an instantaneous negative-going edge occurs at the emitters of Q1 and Q2. This edge will appear at the input of OA2 since the emitter-base diode of Q2 is still forward biased and V_{out} drops correspondingly. This effect is demonstrated by the oscillogram in Figure 7 which shows the emitter voltage of Q1 and Q2. Figure 8 is an oscillogram taken under the same conditions as that in Figure 7, but in this case the rise and fall times of the input waveform have been increased to 40 µs. The slew rate of the amplifier is not a limitation. However, it should be noted that the

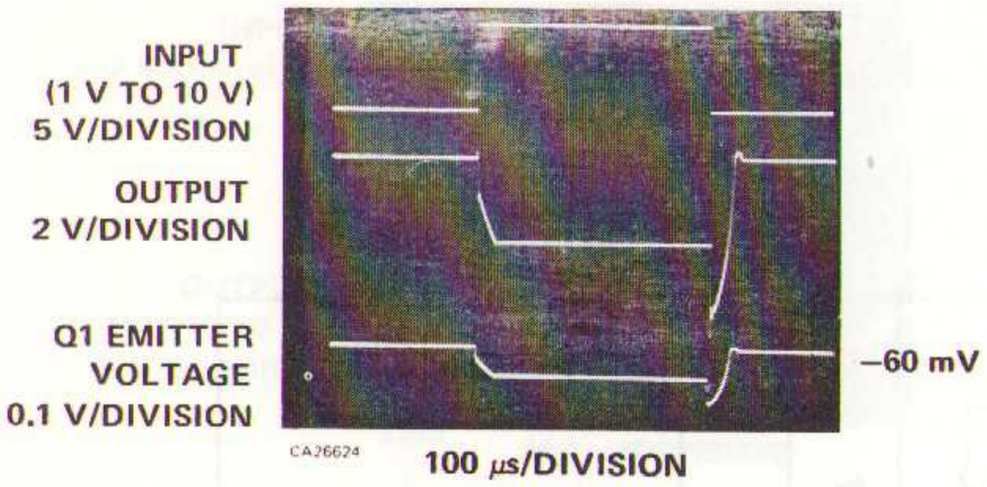

FIGURE 7. Oscillogram Showing the Emitter Voltages of Q1 and Q2

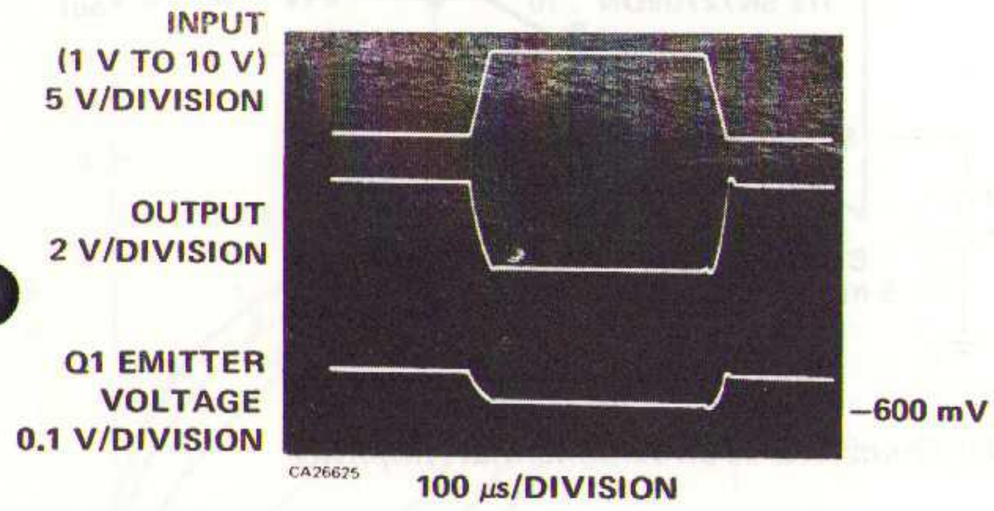

FIGURE 8. Oscillogram Showing Emitter Voltages of Q1 and Q2 When the Rise and Fall Times of the Input Waveform Have Been Increased to 40 µs

settling time of the amplifier when compared with that shown in Figure 6 is not different. Difficulty is likely to be experienced when driving another amplifier (such as the exponential one described later), which could go into saturation when a negative input of 4 or 5 V is applied.

EXPONENTIAL AMPLIFIER

Theory and Practical Considerations

The circuit of the exponential amplifier is shown in Figure 9. This is very similar to the logarithmic circuit except that the collector current is now held constant in the feedback transistor Q3 rather than in the buffer transistor Q4. By analogy with Equation (4) we can write

$$I_{CS4} = I_{CS3} \cdot \{\exp(qV/kT)\} \qquad (10)$$

where I_{CS4} and I_{CS3} are the collector currents of transistors Q4 and Q3 respectively, and where $V = V_{EB4} - V_{EB3} = V_{B4} - V_{B3}$. But as the base of Q4 is grounded, $V_{B4} = 0$ and

$$V = -V_{B3} = V'_{in} \cdot R13/(R12+R13) \qquad (11)$$

The non-inverting input of amplifier OA3 is taken via resistor R18 to the base of transistor Q3. This ensures that the collector-base voltage of Q3 is held at zero which is a condition of the basic relationship in Equation (1). The collector voltage of Q3 will therefore vary in proportion to V_{in}. However, it is assumed that this variation will be small compared with the 10 V supply voltage and that

$$I_{CS3} = V_{ref}/R15 \qquad (12)$$

The current in feedback resistor R14 equals the collector current of transistor Q4 and the output voltage of OA4 is defined by

$$V_o = V_{ref} \cdot \frac{R14}{R15} \cdot \exp\left[-\frac{q}{kT} V_{in} \frac{R13}{R12+R13}\right] \qquad (13)$$

In general, even for matched transistors, I_{O3} and I_{O4} will not be exactly equal. When $I_{CS4} = I_{CS3}$

$$\frac{I_{O3}}{I_{O4}} = \exp\left[q(V_{B4} - V_{B3})/kT\right] = \exp(qV/kT)$$

and there is a small differential offset voltage given by

$$V = \frac{kT}{q} \log_e \frac{I_{O3}}{I_{O4}}$$

For the dual transistor, 2N3680, V is less than 3 mV. The effect of V in the exponential amplifier is to change the slope, (V_{ref} R22/R15). The offset control R16, is provided to enable the effect of V to be set to zero. This is done by making V_{in} equal to 0 and adjusting R16 to give V_o equal to 5.0.

The transfer characteristic of the exponential amplifier is shown in Figure 10. This characteristic has good linearity over more than three decades. The divergences are due to reasons similar to those in the logarithmic amplifier when the bulk resistance of transistor Q4 becomes significant at higher values of collector current. The divergence at the low-voltage end of the characteristic is due to the differential-input offset voltage, of amplifier OA4. Figures 11 to 13 show the responses of the exponential amplifier to input steps of 10 mV to 100 mV, 100 mV to 1 V and 1 V to 10 V respectively. These show a small amount of ringing indicating that the frequency compensation of amplifiers OA3 and OA4 is acceptable. Figure 11 shows a certain amount of noise on the output waveform which starts to become significant at low output voltages. As with the logarithmic amplifier, the effects of slew rate limitation become apparent in Figure 13 where a large output voltage-swing is required.

A POWER LAW SYSTEM

When R13/(R12 + R13) = 1/a and (R1 + R2)/R2 = b, and the exponential amplifier is driven from a logarithmic amplifier we have

$$V_o' = V_{ref}\left[b/a \log_e(V_{in} \cdot R3/R4 \cdot V_{ref})\right] \cdot R14/R15 \qquad (14)$$

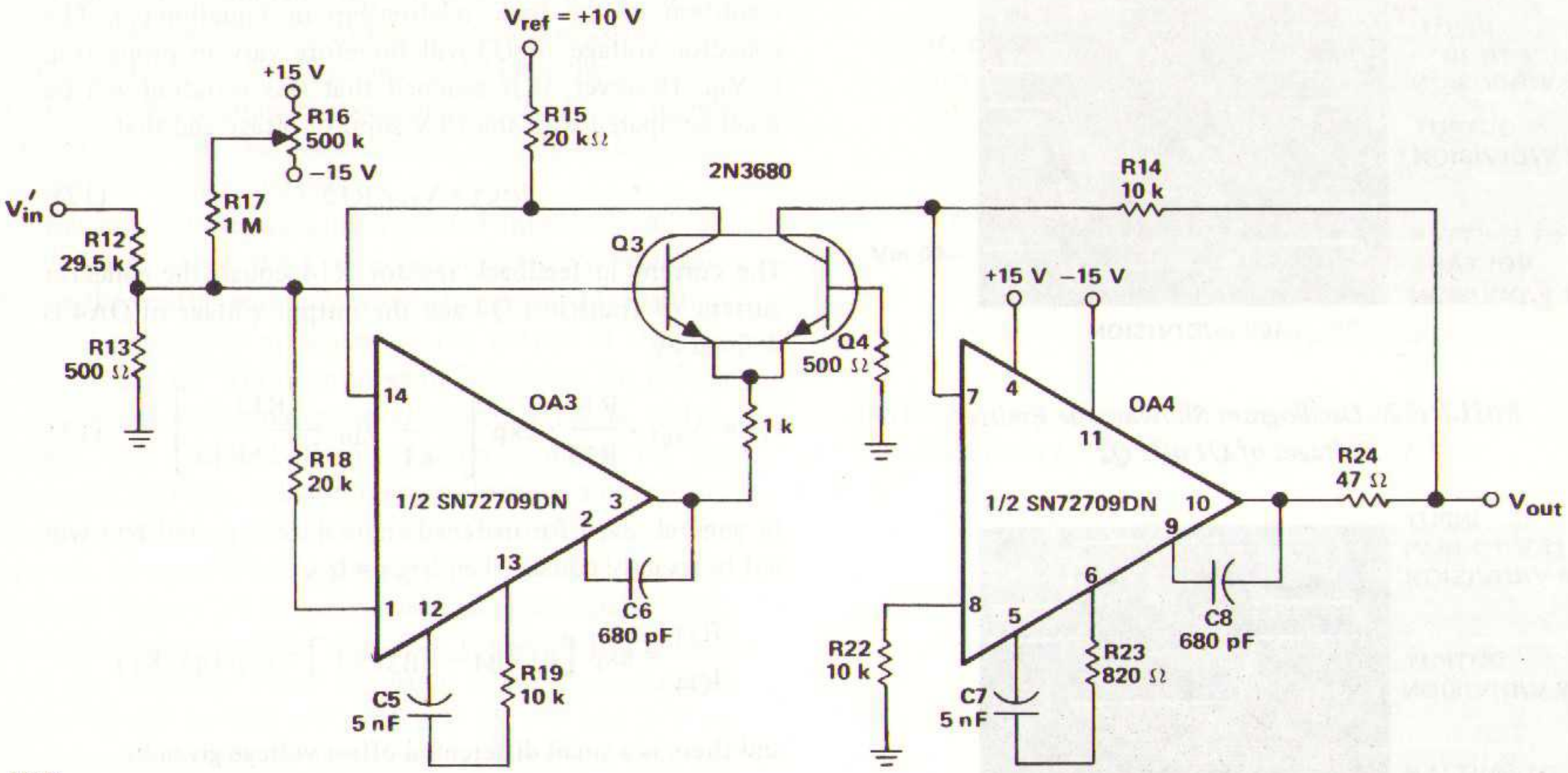

FIGURE 9. Circuit Diagram Showing Two SN72709DN Connected as an Exponential Amplifier

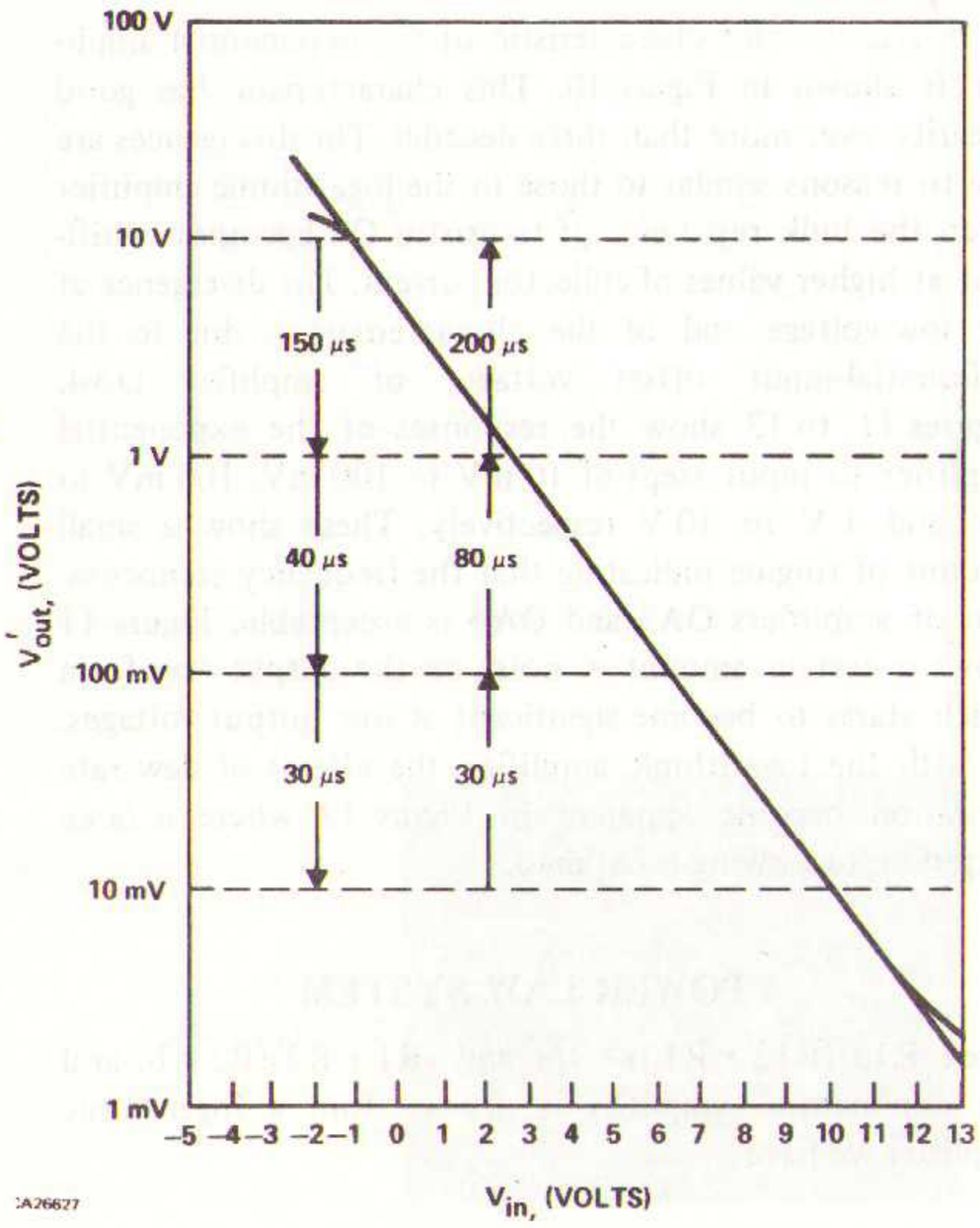

FIGURE 10. Transfer Characteristic of the Exponential Amplifier in Figure 9

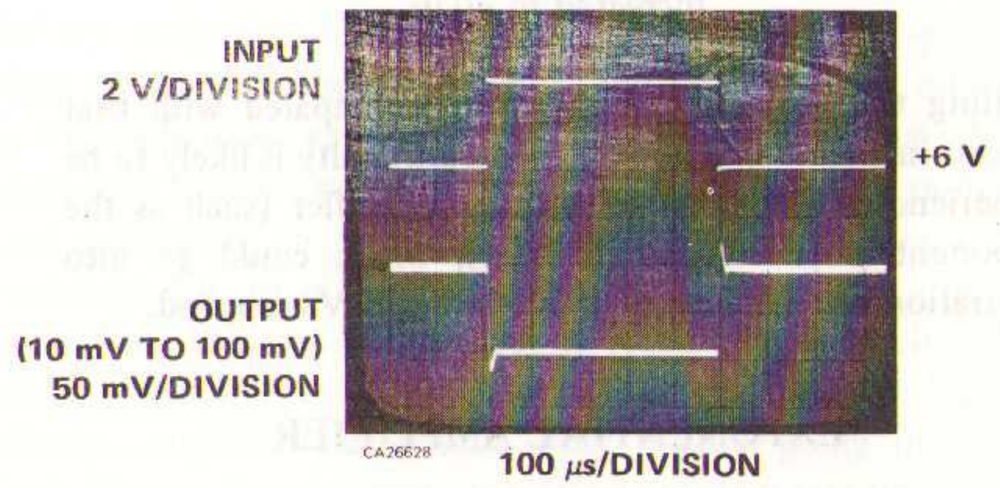

FIGURE 11. Oscillogram Showing Input and Output Waveforms for the Decade 10 mV to 100 mV

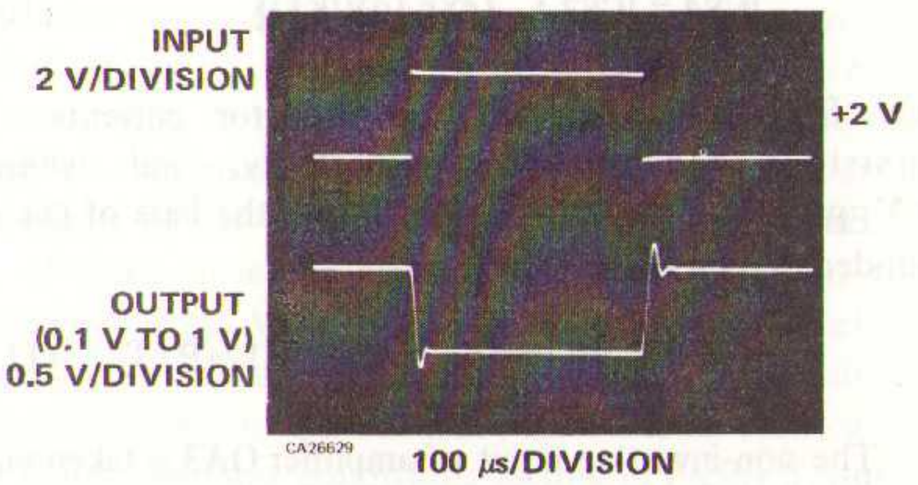

FIGURE 12. Oscillogram Showing Input and Output Waveforms for the Decade 0.1 V to 1 V

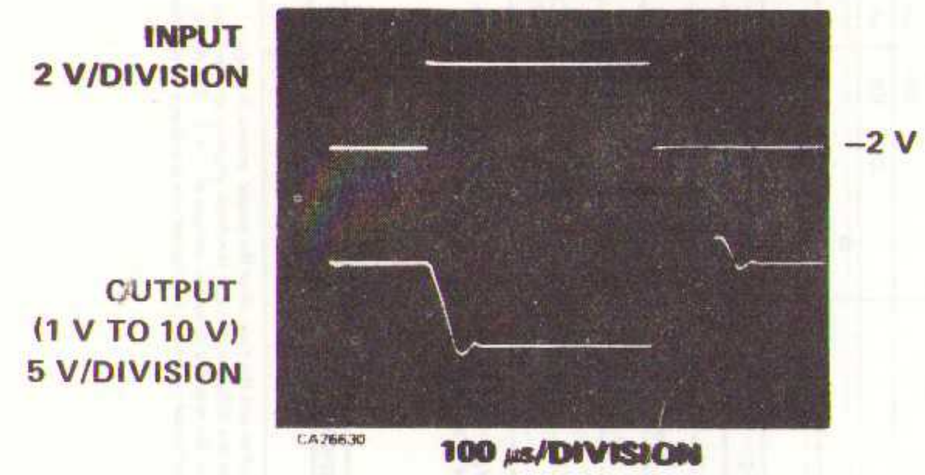

FIGURE 13. Oscillogram Showing Input and Output Waveforms for the Decade 1 V to 10 V

$$= V_{ref} \cdot (V_{in} \cdot R3/R4 \cdot V_{ref})^{b/a} \cdot R14/R15 \qquad (15)$$

Therefore $V_o' = 5(V_{in}/5)^n$ V

where $n = b/a$

Figure 14 shows a range of power-law curves for the function

$$y = x^n$$

where

$$n = \frac{1}{4}, \frac{1}{3}, \frac{1}{2}, 1, 2, 3 \text{ and } 4$$

and where

$$y = \frac{V_o}{5} \quad \text{and} \quad x = \frac{V_{in}}{5}$$

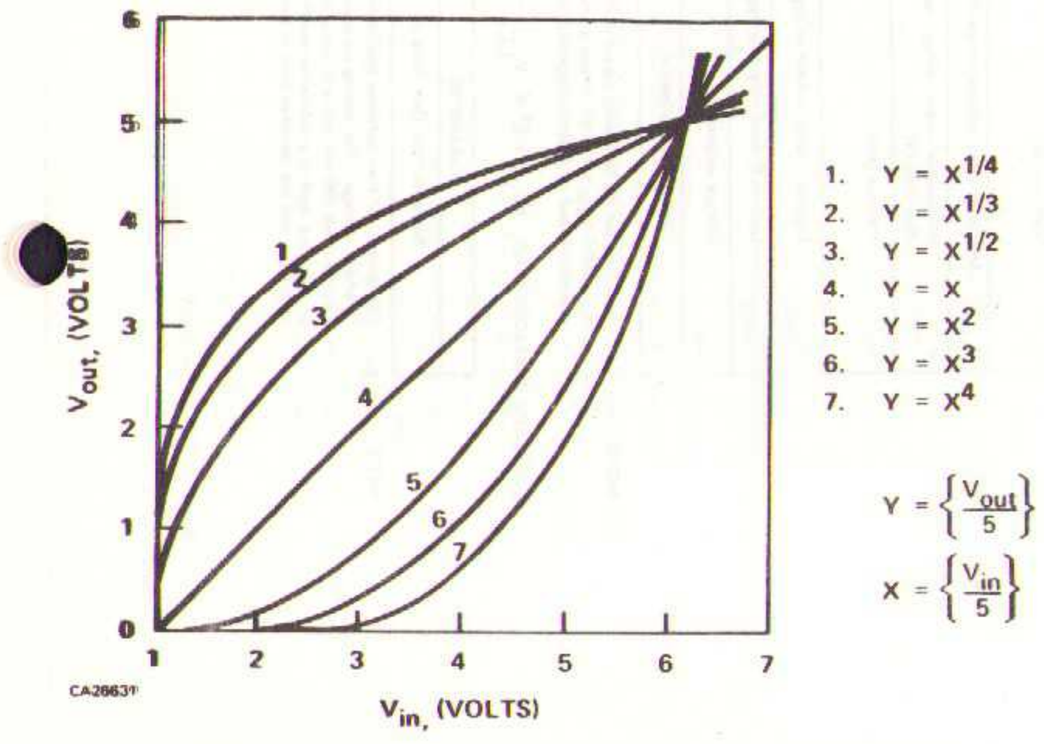

***FIGURE 14.** A Range of Power Law Curves for the Function $y = x^n$ When $n = 1/4, 1/2, 1/3, 1, 2, 3$ and 4*

In order to obtain these powers, resistor R13 was given values of 119.5 k, 89.5 k, 29.5 k, 14.5 k, 9.5 k, 7.0 k respectively.

With more than one logarithmic amplifier in conjunction with an exponential amplifier it is possible to generate products such as $z = xy$ by using the arrangement shown in Figure 15.

Note that when an exponential amplifier is used in conjunction with one or more logarithmic amplifiers to form a power law or multiplier system the transistor pairs should be thermally connected. If this is done the output voltage of the circuit will no longer be a function of ambient temperature T.

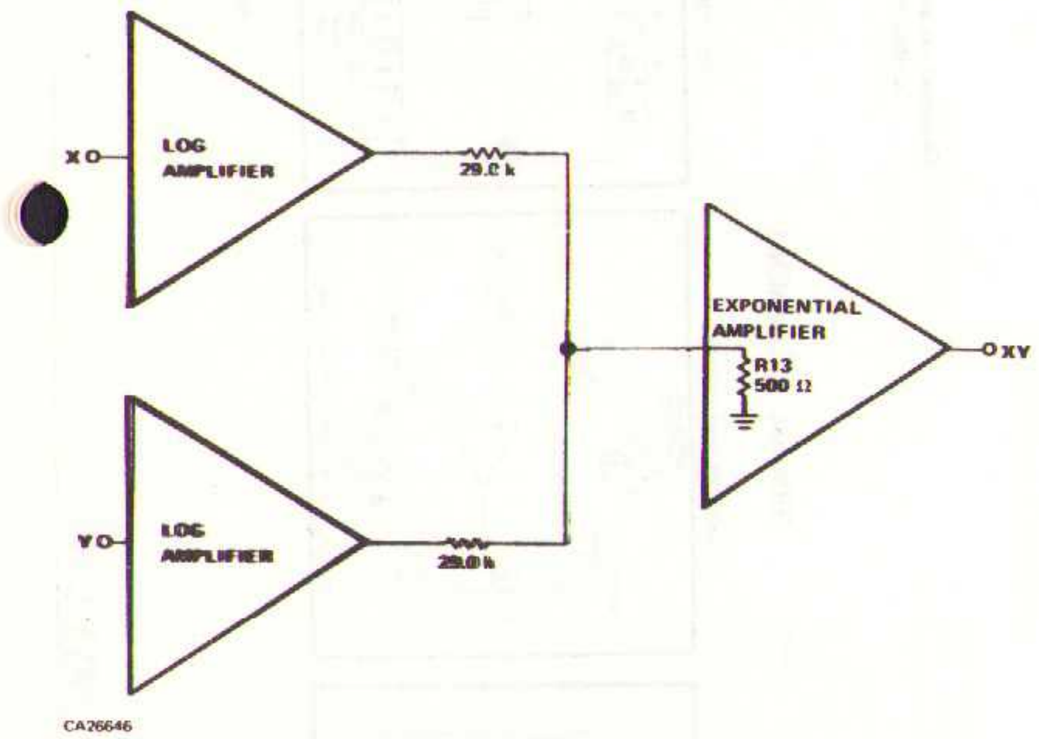

FIGURE 15. Two Logarithmic Amplifiers Used With an Exponential Amplifier to Generate a Product xy

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DIFFERENTIAL VOLTAGE COMPARATORS

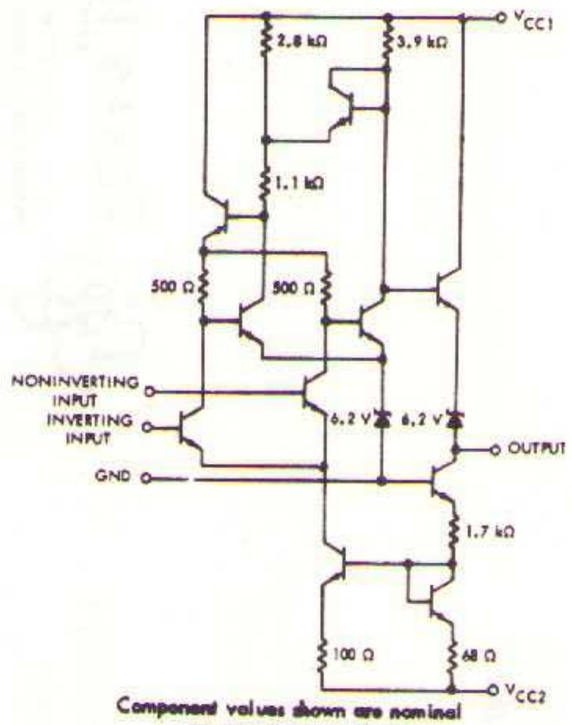
featuring

- Fast Response Times
- Low Offset Characteristics

description

The SN52 710 circuit is a high-speed comparator with differential inputs and a low impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low drift and offset characteristics. This circuit is particularly attractive for applications requiring an amplitude discriminator, memory sense amplifier, or a high-speed voltage comparator. The SN52 710, SN52 710L and SN52 710N are characterized for operation over the temperature range of −55°C to 125°C. The SN72 710, SN72 710L and SN72 710N are characterized for operation from 0°C to 70°C.

Texas Instruments Series 52/72 catalog lines of linear integrated circuits offer higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits.

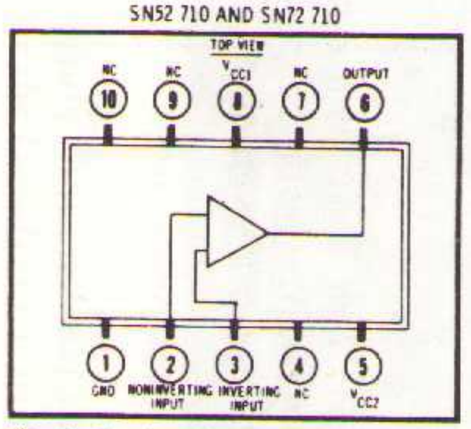


Component values shown are nominal

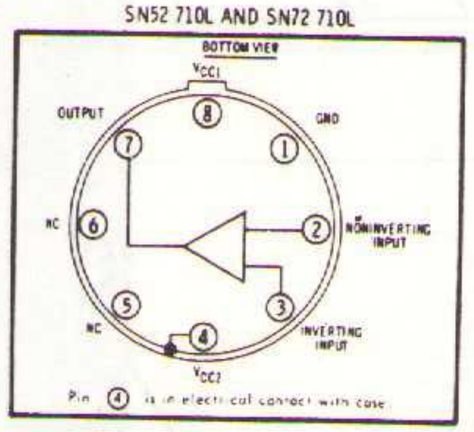
SCHEMATIC DIAGRAM

TERMINAL ASSIGNMENTS

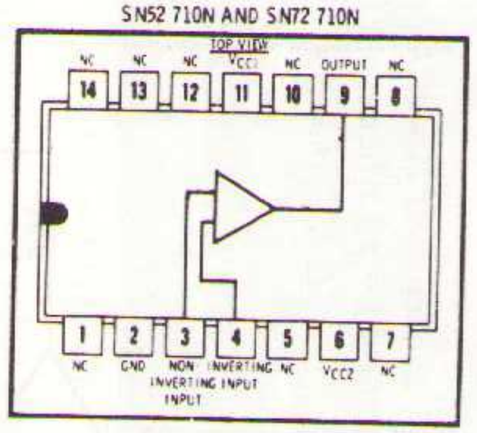
SN52 710 AND SN72 710



SN52 710L AND SN72 710L



SN52 710N AND SN72 710N



NC — No internal connection.

† Patented by Texas Instruments

SC 10320
JULY 1967
REPLACES SC9421A FEBRUARY 1967

TEXAS INSTRUMENTS
INCORPORATED

absolute maximum ratings

Supply Voltages (See Note 1):	V_{CC1}	14 V
	V_{CC2}	−7 V
Differential Input Voltage (See Note 2)		±5 V
Input Voltage (Either Input, See Note 1)		±7 V
Peak Output Current		10 mA
Continuous Total Power Dissipation:	SN72 710 and SN72 710L	200 mW
	SN72 710N	300 mW
Operating Free-Air Temperature Range		0°C to 70°C
Storage Temperature Range:	SN72 710 and SN72 710L	−65°C to 150°C
	SN72 710N	−55°C to 150°C

NOTES:
1. These voltage values are with respect to network ground.
2. These voltage values are with respect to the other input.

electrical characteristics (unless otherwise noted V_{CC1} = 12 V, V_{CC2} = −6 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage	$R_S \le 200\ \Omega$, T_A = 0°C to 70°C			10	mV
		V_{out} = 1.4 V, $R_S \le 200\ \Omega$		2	7.5	mV
α_{VDI}	Differential-input offset voltage temperature coefficient (See Note 7)	T_A = 0°C to 70°C		7.5		μV/deg
I_{DI}	Differential-input offset current (See Note 7)	T_A = 0°C to 70°C			25	μA
		V_{out} = 1.4 V		1	15	μA
I_{in}	Input current	T_A = 0°C to 70°C			150	μA
				25	100	μA
V_{in}	Maximum input voltage range (See Note 1)	V_{CC2} = −7 V	±5			V
$V_{in\ D}$	Differential-input voltage range (See Note 2)		±5			V
A_V	Voltage gain	T_A = 0°C to 70°C	500			
			700	1200		
$V_{out(1)}$	Logical 1 level output voltage	$V_{in\ D} \ge 15$ mV, $I_{load} \le -0.5$ mA	2.5	3.5	4	V
$V_{out(0)}$	Logical 0 level output voltage	$V_{in\ D} \ge 15$ mV, $I_{sink} \le 1.6$ mA	−1	−0.5	0	V
r_{out}	Output resistance			200		Ω
P_T	Total power dissipation			110		mW

NOTE: 7. Specified for the following output voltage levels: when T_A = 0°C V_{out} = 1.5 V, when T_A = 25°C V_{out} = 1.4 V, and when T_A = 70°C V_{out} = 1.2 V. These output voltage levels were selected as they fall within the logic threshold voltage ranges normally found in digital integrated logic circuits.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time (See Note 6)	V_{in} = 100 mV		40		ns

NOTE: 6. The interval of time between application of a 100 mV input step function and the time when the output crosses the logic threshold voltage. For testing purposes, conditions are established at the differential-input terminals whereby an input step function from 100 mV to 0 will cause the output voltage to rise just to the selected threshold voltage of 1.4 V. Conditions on the input used as a reference are then adjusted to cause the 100 mV input to drive 5 mV beyond the previously established conditions and the response time is measured.

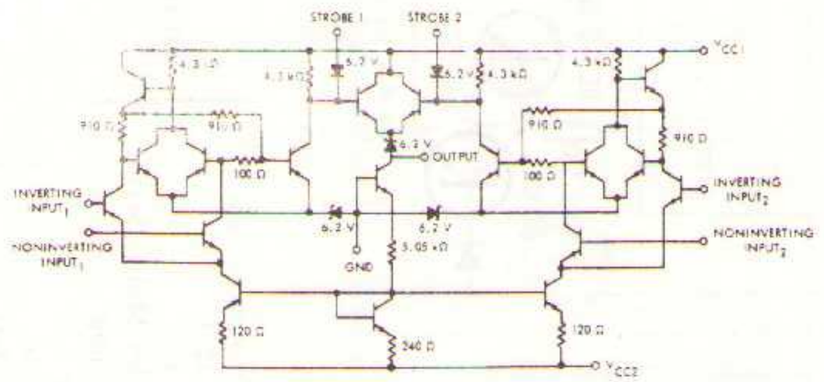
DUAL DIFFERENTIAL VOLTAGE COMPARATORS
featuring

- Fast Response Times
- Low Offset Characteristics

description

The SN52 711 circuit is a high-speed dual comparator with differential inputs and a low impedance output. Component matching, inherent with silicon monolithic circuit fabrication techniques, produces a comparator circuit with low drift and offset characteristics. An independent strobe input is provided for each of the two channels. The comparator output pulse width may be "stretched" by varying the capacitive loading. These dual comparators are particularly attractive for applications requiring an amplitude-discriminating sense amplifier with an adjustable threshold voltage. The SN52 711, SN52 711L and SN52 711N are characterized for operation over the temperature range of −55°C to 125°C. The SN72 711, SN72 711L and SN72 711N are characterized for operation from 0°C to 70°C.

Texas Instruments Series 52/72 catalog lines of linear integrated circuits offer higher reliability, lower cost, smaller size, and less weight than equivalent discrete component circuits.

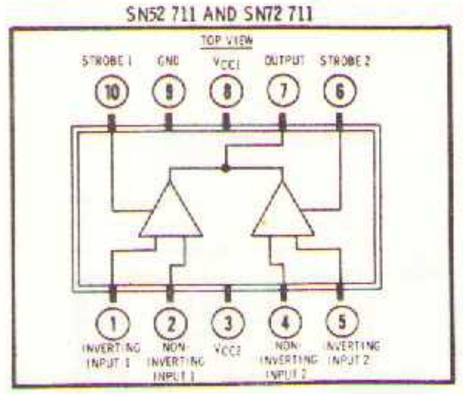


Component values shown are nominal

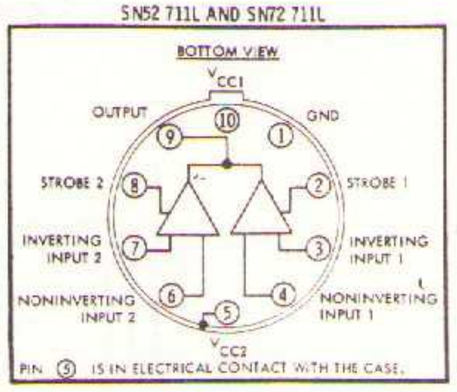
SCHEMATIC DIAGRAM

TERMINAL ASSIGNMENTS

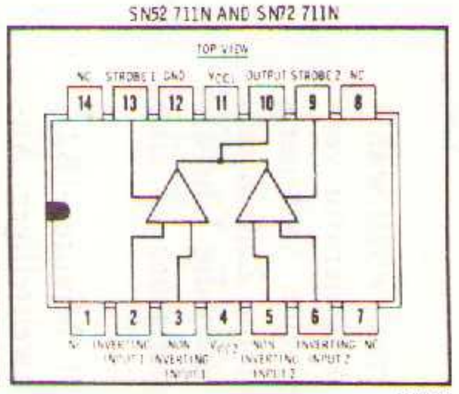
SN52 711 AND SN72 711



SN52 711L AND SN72 711L



SN52 711N AND SN72 711N



NC — No internal connection
† Patented by Texas Instruments

SC10027
MARCH 1968
REPLACES SC9427A FEBRUARY 1967

TEXAS INSTRUMENTS

absolute maximum ratings

Supply Voltages (See Note 1):	V_{CC1}	14 V
	V_{CC2}	−7 V
Differential Input Voltage (See Note 2)		±5 V
Input Voltage (Either Input, See Note 1)		±7 V
Strobe Input Voltage		6 V
Peak Output Current		50 mA
Continuous Total Power Dissipation		300 mW
Operating Free-Air Temperature Range		0°C to 70°C
Storage Temperature Range:	SN72 711 and SN72 711L	−65°C to 150°C
	SN72 711N	−55°C to 150°C

NOTES: 1. These voltage values are with respect to network ground.
2. These voltage values are with respect to the other input.

electrical characteristics (unless otherwise noted V_{CC1} = 12 V, V_{CC2} = −6 V, T_A = 25°C)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DI}	Differential-input offset voltage (See Note 7)	$R_S \le 200\ \Omega$, $V_{CMI} = 0$, T_A = 0°C to 70°C			6	mV
		$R_S \le 200\ \Omega$, T_A = 0°C to 70°C			10	mV
		V_{out} = 1.4 V, $R_S \le 200\ \Omega$, $V_{CMI} = 0$		1	5	mV
		V_{out} = 1.4 V, $R_S \le 200\ \Omega$		1	7.5	mV
α_{VDI}	Differential-input offset voltage temperature coefficient	T_A = 0°C to 70°C		5		μV/deg
I_{DI}	Differential-input offset current (See Note 7)	T_A = 0°C to 70°C			25	μA
		V_{out} = 1.4 V		0.5	15	μA
I_{in}	Input current	T_A = 0°C to 70°C			150	μA
				25	100	μA
$I_{in\ S}$	Strobe input current	$V_{in\ S} = 0$		−1.2	−2.5	mA
V_{in}	Maximum input voltage range (See Note 1)	V_{CC2} = −7 V	±5			V
$V_{in\ D}$	Differential-input voltage range (See Note 2)		±5			V
A_V	Voltage gain	T_A = 0°C to 70°C	500			
			700	1500		
$V_{out(1)}$	Logical 1 level output voltage	$V_{inD} \ge 10$ mV		4.5	5	V
		$V_{inD} \ge 10$ mV, I_{load} = −5 mA	2.5	3.5		V
$V_{out(0)}$	Logical 0 level output voltage	$V_{in\ D} \ge 10$ mV	−1	−0.5	0	V
		$V_{in\ S} \le 0.3$	−1		0	V
I_{sink}	Output sink current	$V_{in\ D} \ge 10$ mV, $V_{out} \le 0$	0.5	0.8		mA
r_{out}	Output resistance			200		Ω
I_{CC1}	V_{CC1} supply current	$V_{out} \le 0$		8.6		mA
I_{CC2}	V_{CC2} supply current			−3.9		mA
P_T	Total power dissipation			130	230	mW

NOTE 7: Specified for the following output voltage levels: when T_A = 0°C V_{out} = 1.5 V, when T_A = 25°C V_{out} = 1.4 V, and when T_A = 70°C V_{out} = 1.2 V. These output voltage levels were selected as they fall within the logical threshold voltage ranges found in some digital integrated logic circuits.

switching characteristics, V_{CC1} = 12 V, V_{CC2} = −6 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Response time (See Note 6)	V_{in} = 100 mV		40		ns
Strobe release time			12		ns

NOTE 6: The interval of time between application of a 100 mV input step function and the time when the output crosses the logic threshold voltage. For testing pruposes, conditions are established at the differential input terminals whereby an input step function from 100 mV to 0 will cause the output voltage to rise just to the selected threshold voltage of 1.4 V. Conditions on the input used as a reference are then adjusted to cause the 100 mV input to drive 5 mV beyond the previously established conditions and the response time is measured.

Komplexe Bausteine der Serie FL 100 in einer Uhr mit digitaler Anzeige

Von Helmut Liedl und Walter Spichall

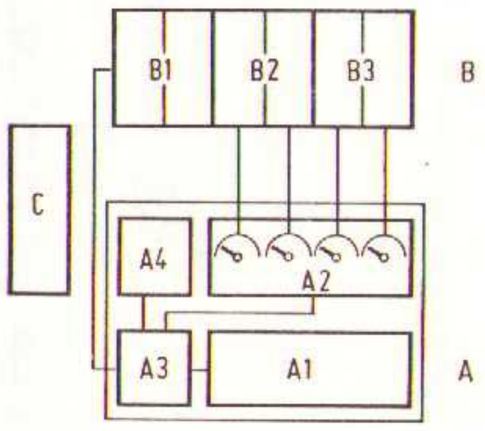
Die für einen universellen Einsatz vorgesehenen Logikserien wurden in den letzten Jahren ständig erweitert und ausgebaut. Die bessere Beherrschung der technologischen Verfahren machte es möglich, immer mehr Bauelemente gemeinsam herzustellen und den Funktionsumfang integrierter Schaltungen zu vergrößern. Man faßte Verknüpfungsglieder zu Flipflop-Speichergliedern verschiedenster Form zusammen und diese wiederum zu Grundbaugruppen, beispielsweise zu Zählern und Schieberegistern. Diese sogenannten MSI-(Medium Scale Integration-)Bausteine eröffnen dem Entwickler bei der Konzipierung der Geräte neue Wege und ermöglichen ihm einen wirtschaftlichen Aufbau von umfangreichen Gerätefunktionen mit nur wenigen Bauelementen. Ein Beispiel für den Einsatz der zur Zeit wohl wichtigsten MSI-Bausteine — Zähler und Decoder-Treiber — ist die Uhr mit digitaler Anzeige.*

Wirkungsweise einer Uhr mit digitaler Anzeige

Das in Bild 1 gezeigte Blockschaltbild einer Uhr mit digitaler Anzeige enthält außer dem Netzteil (C) eine Steuereinheit (A) und eine Zähleinheit (B).

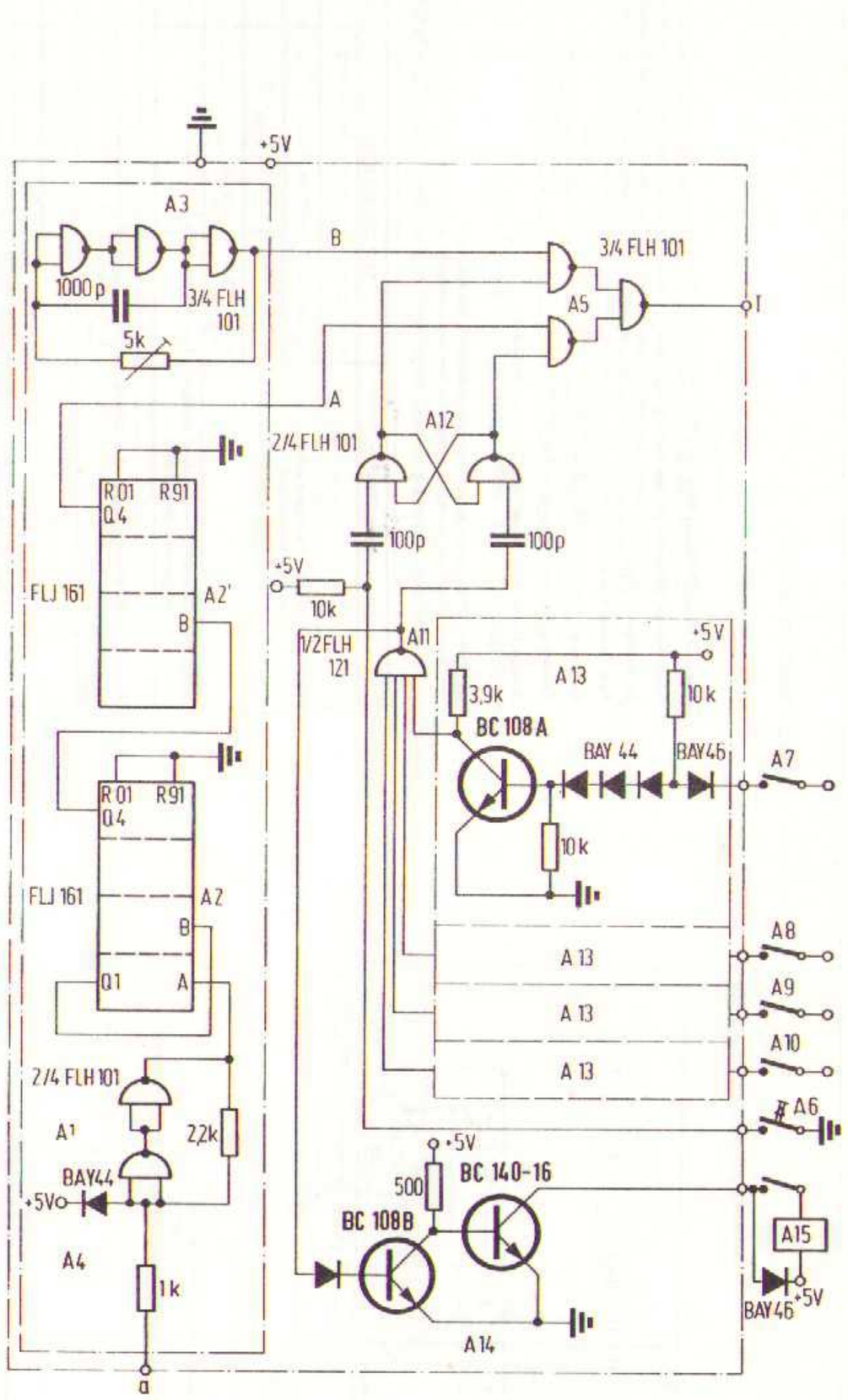
In der Steuereinheit befinden sich das Zeitnormal, wozu wahlweise die 50-Hz-Netzfrequenz oder ein Quarzgenerator verwendet werden kann, und die Aufbereitung zum Ansteuern der Zähleinheit, ferner eine Einrichtung für die Zeiteinstellung und für die Signalgewinnung, wenn man die Uhr als Wecker benutzen will. Als akustischer Signalgeber ist eine Schnarre vorgesehen.

Die Zähleinheit besteht aus Sekunden-(B1-), Minuten-(B2-) und Stunden-(B3-)Einheiten mit jeweils zweistelliger Anzeige.



A Steuereinheit
A1 Zeitnormal, A2 Vorwahlschalter, A3 Schalteinheit,
A4 Wecker
B Zähleinheit
B1 Sekunden, B2 Minuten, B3 Stunden
C Netzteil

Bild 1 Blockschaltbild einer Uhr mit digitaler Anzeige



A1	Impulsformer	50-Hz-Zeitnormal
A2	Teiler 10:1	
A2'	Teiler 5:1	
A3	Astabiler Multivibrator	
A4	Anpassung	
A5	Weiche	
A6	Stelltaste	
A7 bis A10	Vorwahlschalter	
A11	NAND-Glied	
A12	Steuer-Flipflop	
A13	Pegelanpassung	
A14	Schnarrenansteuerung	
A15	Schnarre	

Bild 2 Schaltung der Steuereinheit A in Bild 1 mit 50-Hz-Netzfrequenz als Zeitnormal

* Weitere komplexe Bausteine der Serie FL 100 sind der 4-Bit-Binärzähler FLJ 181, das 4-Bit-Rechts-Links-Schieberegister FLJ 191, der Dezimal-Vorwärts-Rückwärts-Zähler FLJ 201, der Binär-Vorwärts-Rückwärts-Zähler FLJ 211, das 8-Bit-Schieberegister FLJ 221, das 4-Bit-Schieberegister FLJ 231, der Dezimal-Vorwärts-Rückwärts-Zähler mit Rückstellung FLJ 241 und der Binär-Vorwärts-Rückwärts-Zähler mit Rückstellung FLJ 251.

Steuereinheit mit 50-Hz-Netzfrequenz

Bild 2 zeigt die Schaltung einer Steuereinheit, die als Zeitnormal die 50-Hz-Netzfrequenz verwendet. Die erforderliche Wechselspannung wird dem Netzteil entnommen und mit einem aus zwei NAND-Gliedern aufgebauten Impulsformer (A1) zu 20-ms-Rechteckimpulsen umgeformt. Diese Impulse werden einem Teiler 50:1 zugeführt, der an seinem Ausgang A Sekundenimpulse abgibt. Der Teiler besteht aus zwei dekadischen Binärzählern FLJ 161, von denen der eine (A2) als Teiler 10:1, der andere (A2′) als Teiler 5:1 geschaltet ist.

Ein ebenfalls mit NAND-Gliedern aufgebauter astabiler Multivibrator (A3) liefert an seinem Ausgang B eine Hilfsfrequenz von etwa 100 kHz für das Stellen der Uhr.

Sowohl die Sekundenimpulse als auch die Hilfsfrequenz werden einer Weiche (A5) zugeführt, deren Ausgang T die Zähleinheit speist. Welche Frequenz als Taktfrequenz in die Zähleinheit einläuft, bestimmt ein aus NAND-Gliedern aufgebautes Steuer-Flipflop (A12).

Zum Stellen der Uhr — der Stellvorgang wird durch Drücken einer Taste (A6) eingeleitet — läßt die Weiche die 100-kHz-Hilfsfrequenz passieren. Die Zähleinheit läuft auf die mit den Vorwahlschaltern (A7 bis A10) eingestellte Zeit. Über die Vorwahlschalter, die mit den Anzeigeröhren für Minuten und Stunden verbunden sind, wird mit einem NAND-Glied (A11) ein Stoppsignal erzeugt, das das Steuer-Flipflop (A12) wieder in die andere Lage kippt. Die Uhr zählt nach Erreichen der vorgewählten Zeit im Sekundenrhythmus weiter. Der Einstellvorgang ist in einer Sekunde abgeschlossen.

Das Signal liegt am Ausgang des NAND-Gliedes (A11) eine Minute an und steuert auch die Schnarre an. Die Weckzeit wird also ebenfalls mit den Vorwahlschaltern (A7 bis A10) eingestellt. Zwei Transistoren erzeugen die für die Schnarre erforderliche Ansteuerleistung.

Steuereinheit mit 100-kHz-Quarzschaltung

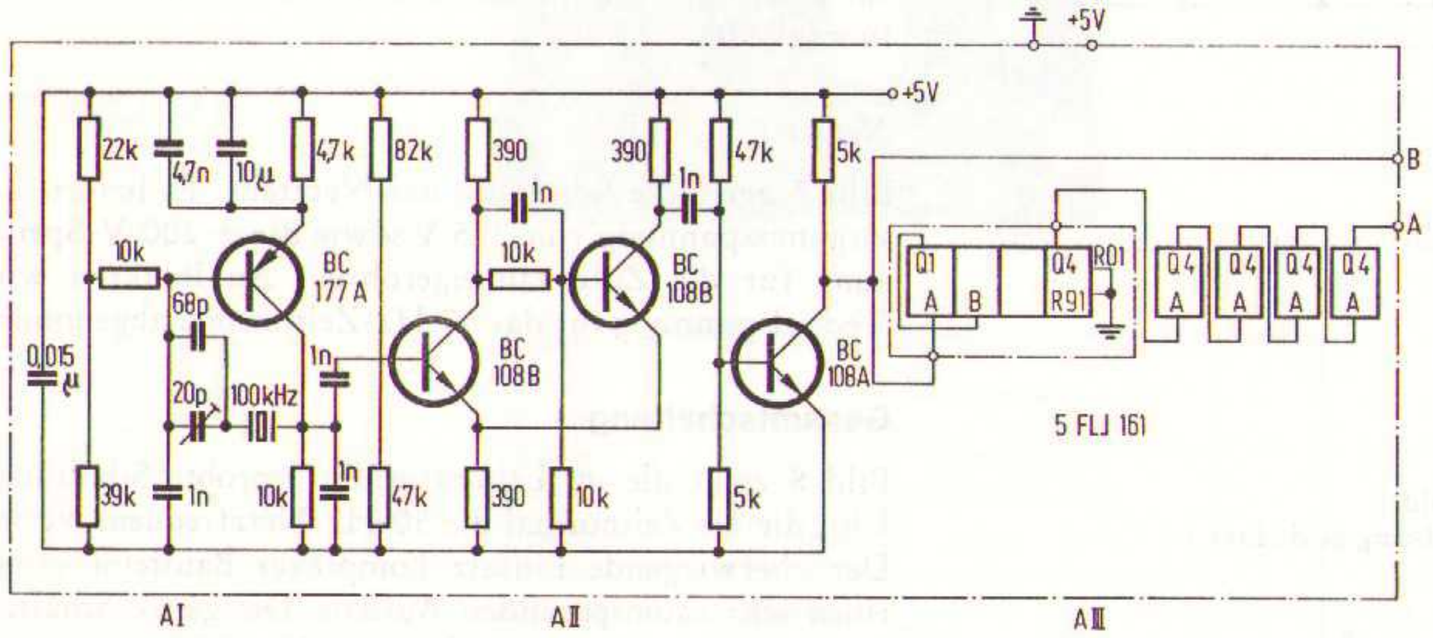
Eine Quarzschaltung als Zeitnormal ermöglicht es, eine wesentlich genauere Zeitanzeige zu erreichen als mit der 50-Hz-Netzfrequenz. Bild 3 zeigt die Schaltung eines quarzstabilisierten 100-kHz-Zeitnormals. Es besteht aus einem Oszillator (AI), einem Impulsformer (AII) und einem Frequenzteiler (AIII). Zum Erzeugen von Sekundenimpulsen am Ausgang A muß man die Oszillatorfrequenz im Verhältnis 100 000:1 untersetzen. Dies wird mit fünf dekadischen Binärteilern FLJ 161 erreicht.

Zum Stellen der Uhr kann die Oszillatorfrequenz direkt verwendet werden. Eine Hilfsschaltung wie beim 50-Hz-Zeitnormal ist nicht erforderlich.

Zähleinheit

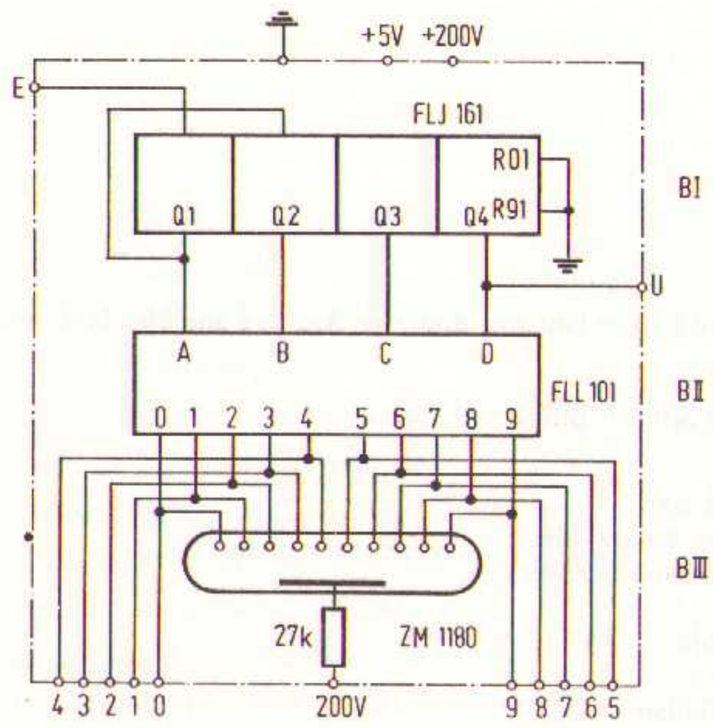
In der Zähleinheit werden die von der Steuereinheit gelieferten Impulse gezählt und angezeigt. Die Anzeige ist sechsstellig; angezeigt werden Sekunden, Minuten und Stunden.

Im Sekunden- und Minutenbereich muß jeweils bis 60 gezählt werden. Die Zähler B1 und B2 (Bild 1) bestehen deshalb aus einer Dekade (Bild 4) — aufgebaut aus einem dekadischen Binärzähler FLJ 161 (BI), einem Decoder-Treiber FLL 101 (BII) und einer Ziffernanzeigeröhre (BIII) — und einer Sextade (Bild 5).



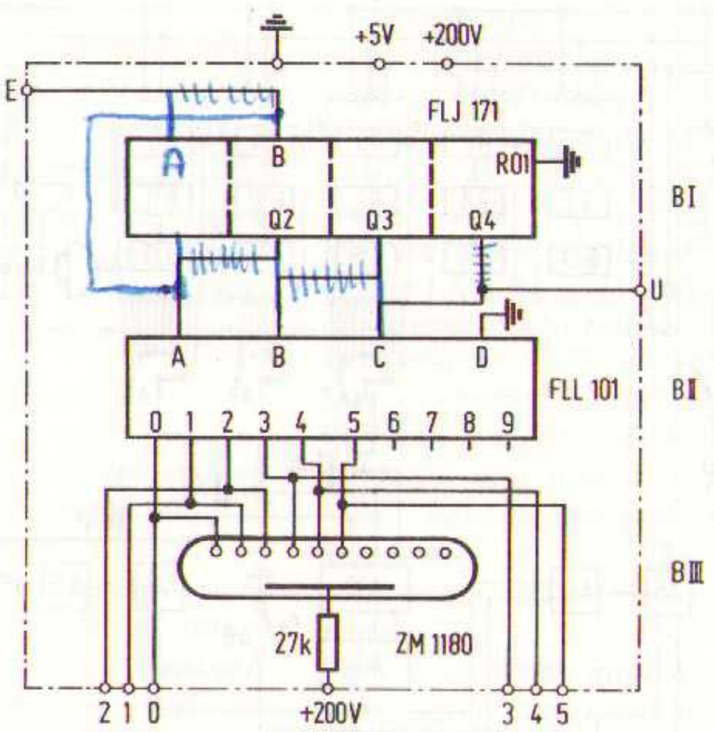
AI Oszillator
AII Impulsformer
AIII Teiler 100 000:1

Bild 3 Schaltung eines quarzstabilisierten 100-kHz-Zeitnormals der Steuereinheit A in Bild 1



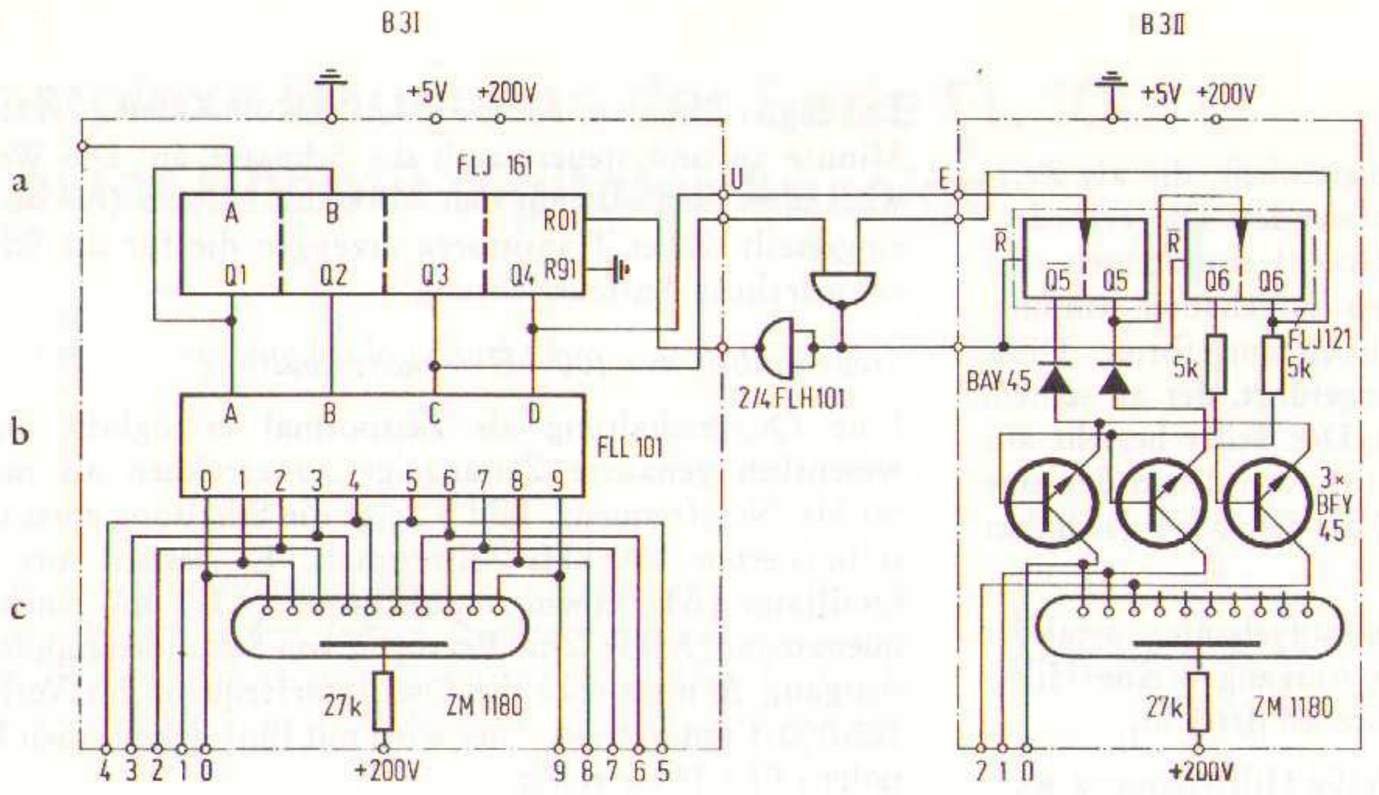
BI Dekadischer Binärzähler
BII Decoder-Treiber
BIII Ziffernanzeigeröhre

Bild 4
Dekade der Zähleinheit B in Bild 1



BI mod-6-Zähler
BII Decoder-Treiber
BIII Ziffernanzeigeröhre

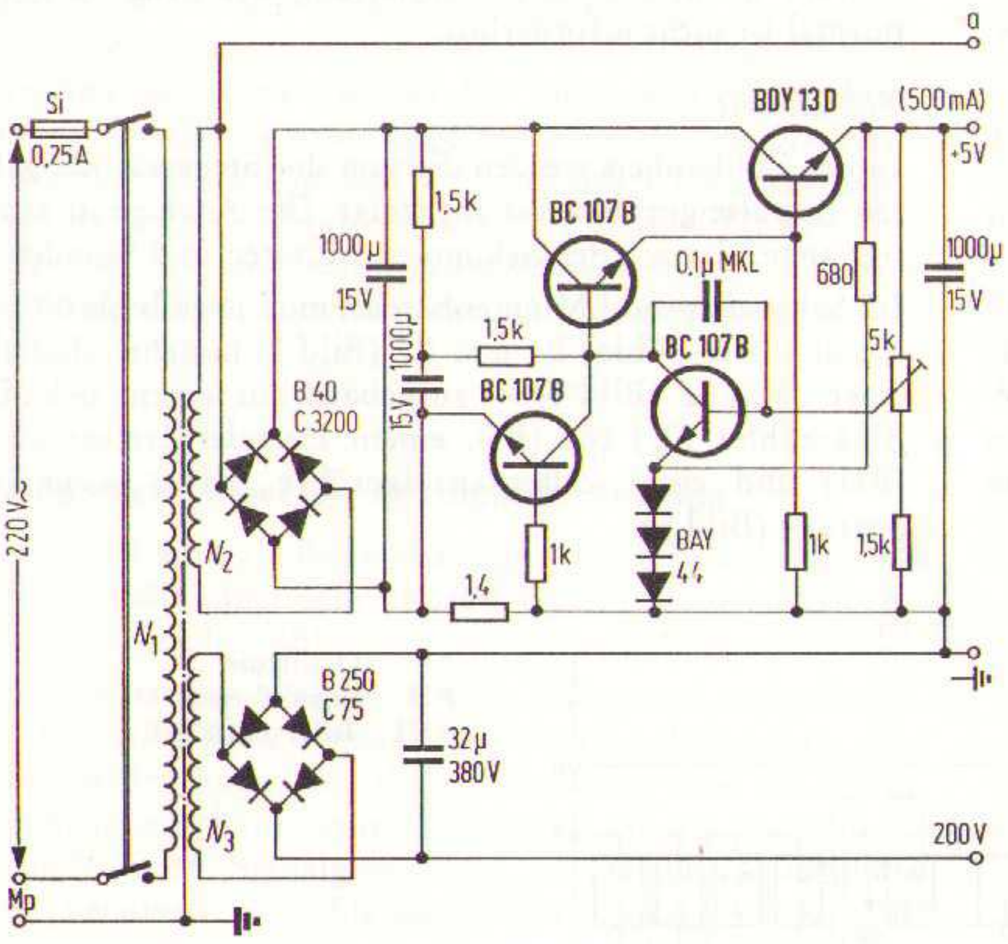
Bild 5
Sextade der Zähleinheit B in Bild 1



B3I Dekade
B3II Triade

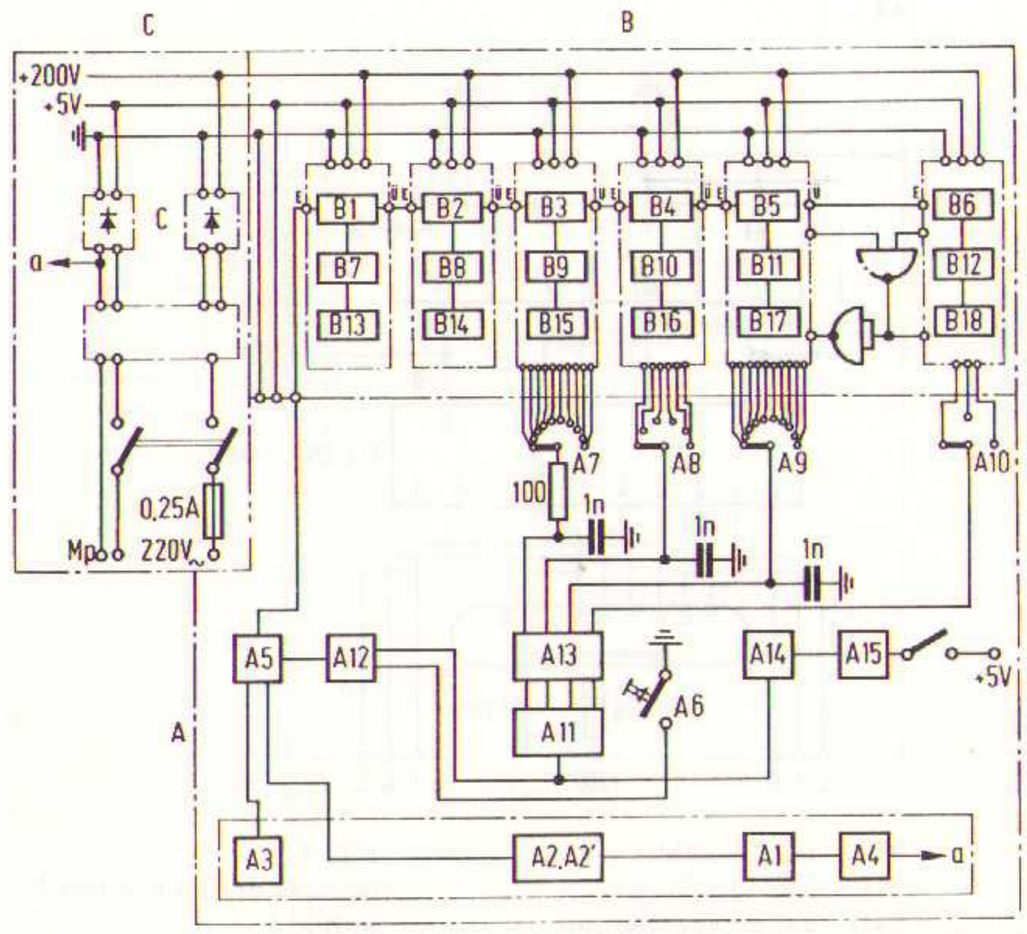
Bild 6 Schaltung des Stundenzählers B3
der Zähleinheit B in Bild 1

a Zähler
b Decoder-Treiber
c Ziffernanzeigeröhre



N_1 = 1560 Wdgn. 0,25 CuL
N_2 = 69 Wdgn. 0,75 CuL
N_3 = 1150 Wdgn. 0,14 CuL

Bild 7 Schaltung des Netzteils C in Bild 1
Transformator M65 Dyn BI IV, wechselseitig geschichtet



Für den mod-6-Zähler der Sextade läßt sich der komplexe Baustein FLJ 171 verwenden, der eine Teilung 12:1 ermöglicht. Der nachfolgende Decoder-Treiber FLL 101 (BII) hat hier nur die Ziffern 0 bis 5 zu decodieren; der Eingang D des Decoders ist deshalb mit »O«-Potential (Masse) verbunden.

Bild 6 zeigt die Schaltung des aus einer Dekade (B3I), ähnlich Bild 4, und einer Triade (B3II) bestehenden Stundenzählers B3. Aus wirtschaftlichen Gründen wurde in der Triade auf den Einsatz des Decoder-Treiber-Bausteins FLL 101, der auch hier durchaus möglich wäre, verzichtet. Weil nur die Ziffern 0 bis 2 angezeigt werden müssen, benötigt man nur wenige Einzelbauelemente. Die Besonderheit der Stundeneinheit besteht darin, daß nach Erreichen der Zahl 23 eine Rückstellung auf 0 erfolgen muß. Zum Rückstellen dienen zwei Verknüpfungsglieder.

Netzteil

Bild 7 zeigt die Schaltung des Netzteils. Es liefert die Versorgungsspannung von + 5 V sowie die + 200-V-Speisespannung für die Ziffernanzeigeröhren. An Punkt a wird die Wechselspannung für das 50-Hz-Zeitnormal abgenommen.

Gesamtschaltung

Bild 8 zeigt die im Laboratorium erprobte Schaltung einer Uhr, die als Zeitnormal die 50-Hz-Netzfrequenz verwendet. Der überwiegende Einsatz komplexer Bausteine ermöglicht einen sehr raumsparenden Aufbau. Die ganze Schaltung erforderte nur 18 Bausteine der Serie FL 100.

Bild 8 Schaltbild einer Uhr mit digitaler Anzeige und 50-Hz-Zeitnormal

A Steuerung
A1 bis A15 wie bei Bild 2

B Zähler
B1, B3 und B5:
Dekadischer Binärzähler;
B2 und B4: mod-6-Zähler;
B6:
mod-3-Zähler
B7 bis B 12:
Decoder-Treiber
B13 bis B18:
Ziffernanzeigeröhren (1 s, 10 s, 1 min, 10 min, 1 h, 10 h)

C Netzteil

Maak zelf een ruitenwisser-regelaar

van dam
ELEKTRONICA

Iedere automobilist weet, dat als het motregent en de voorruit nauwelijks nat is, het zicht er niet veel beter op wordt als men de ruitenwisser in werking stelt. Beter is het de ruitenwisser met tussenpozen van een aantal seconden steeds één slag te laten maken. Dat betekent echter, dat men als maar de schakelaar aan en af moet zetten.

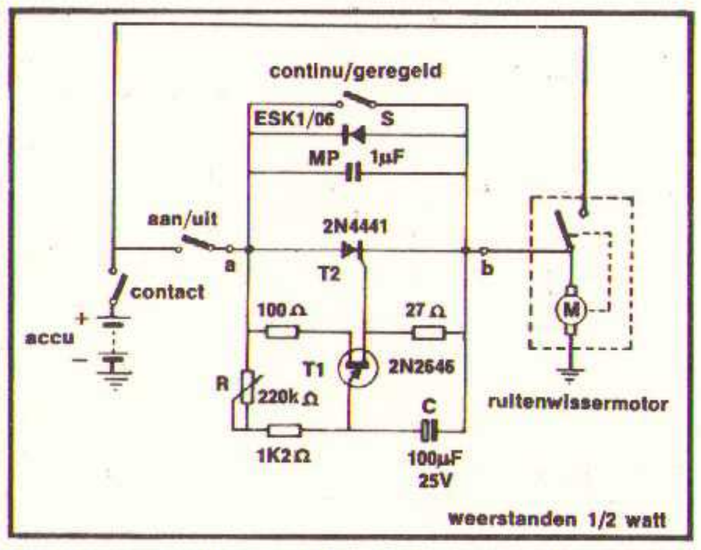
Bouwset

Voor wie van knutselen houdt is het misschien wel aantrekkelijk zelf 'n elektronische interval-schakelaar te bouwen, waarmee het mogelijk is, de ruitenwisser automatisch met tussenpozen — instelbaar van 1 tot 60 seconden — telkens één slag te laten maken.

v. DAM heeft voor dit apparaatje een bouwset beschikbaar, welke op aanvraag onder rembours wordt toegezonden. De kosten bedragen fl. 22,50.

Het is een universele schakeling, die zowel voor 6 als 12 Volts installaties kan worden toegepast, ongeacht of de plus- dan wel de min-pool van de accu met massa is verbonden.

Tot de set behoort een gedrukte bedrading volgens nevenstaand schema en alle tussen de punten a en b aangegeven onderdelen.



De trek-drukschakelaar S en de regelweerstand R zijn gecombineerd uitgevoerd. Dit onderdeel wordt in het dashbord gemonteerd en via soepele draden met de „print" verbonden.

Werking

Zoals U weet keren, na het uitschakelen van een ruitenwisser, de armen altijd in hun eindstand terug. Hiertoe is in de ruitenwissermotor een schakelaartje aangebracht dat de contacten van de ruitenwisserschakelaar overbrugt, als de wisserbladen uit hun ruststand zijn. Van dit systeem is bij onze regelaar gebruik gemaakt. Als de schakelaar S openstaat (regelstand) en de aan-uit schakelaar wordt gesloten, komt de regelaar via de motor onder spanning te staan.

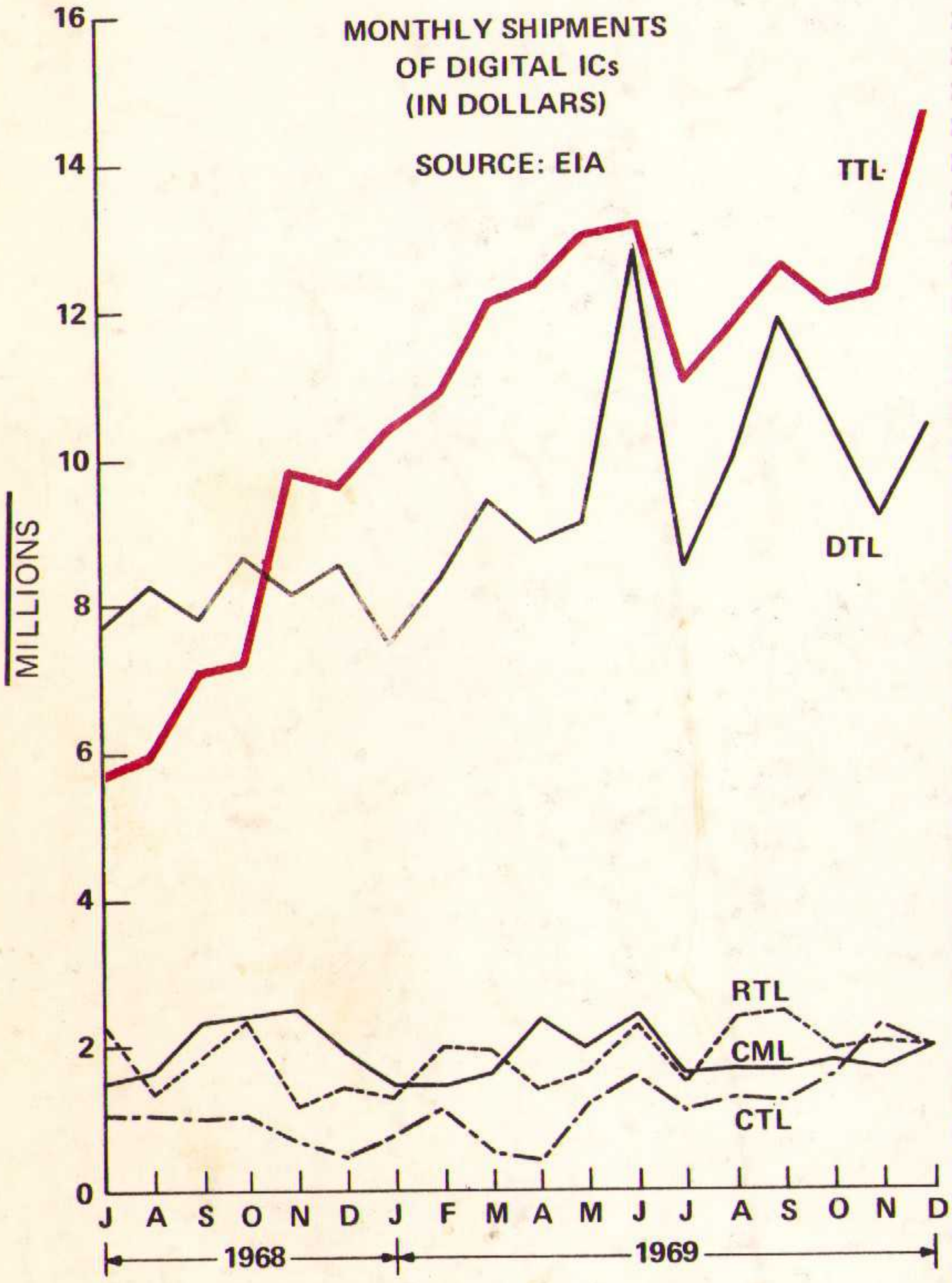
De condensator C wordt nu al naar gelang de stand van regelweerstand R vlug of langzaam opgeladen. Als na enige tijd de condensatorspanning hierbij een bepaalde waarde heeft bereikt komt de transistor T1 in werking en geeft stroom op de „poort" van de thyristor T2.

Deze wordt hierdoor geleidend en schakelt de volle accuspanning op de ruitenwisser. Als de overbruggingsschakelaar op de wissermotor zich sluit wordt de regelaar kortgesloten. De wisserarmen komen in hun eindstand en de motor stopt. Daarna herhaalt het spel zich. Het schema geeft duidelijk aan hoe de regelaar in de auto moet worden aangesloten.

Men kan het beste de draad, welke van schakelaar naar wissermotor loopt, loskoppelen.

Punt a verbindt men nu met het vrijgekomen schakelaarkontakt, punt b met de losgekoppelde draad.

Bij auto's met plus aan massa is deze volgorde juist omgekeerd.



TTL

exclusief BTW in Hfl en DM

	1 - 9	10 - 24	25 - 99	100 up
SN7400N	3,98	3,07	2,69	2,24
SN7402N	3,98	3,07	2,69	2,24
SN7404N	4,55	3,77	3,30	2,75
SN7406N	7,78	6,45	5,64	4,69
SN7408N	3,80	3,14	2,75	2,29
SN7410N	3,98	3,07	2,69	2,24
SN7413N	5,36	4,45	3,88	3,23
SN7420N	3,98	3,07	2,69	2,24
SN7425N	7,18	5,95	5,20	4,33
SN7426N	3,80	3,14	2,75	2,29
SN7430N	3,98	3,07	2,69	2,24
SN7440N	3,96	3,28	2,88	2,38
SN7441AN	zie SN 74141			
SN7442N	17,45	14,40	12,60	10,50
SN7446N	28,40	23,50	20,50	17,10
SN7450N	3,98	3,07	2,69	2,24
SN7451N	3,98	3,07	2,69	2,24
SN7453N	3,98	3,07	2,69	2,2
SN7454N	3,98	3,07	2,69	2,24
SN7460N	3,98	3,07	2,69	2,24
SN7470N	6,72	5,55	4,86	4,05
SN7472N	5,28	4,38	3,82	3,18
SN7473N	8,70	7,15	6,25	5,22
SN7474N	7,75	6,35	5,58	4,65
SN7475N	12,20	10,10	8,85	7,35
SN7476N	9,05	7,46	6,55	5,45
SN7480N	11,80	9,75	8,50	7,10
SN7482N	17,45	14,40	12,60	10,50
SN7483N	26,25	21,70	19,00	15,80
SN7486N	7,90	6,50	5,70	4,75
SN7490N	14,30	11,80	10,35	8,60
SN7491AN	19,25	15,90	13,90	11,60
SN7492N	15,10	12,50	10,95	9,10
SN7493N	15,10	12,50	10,95	9,10
SN7494N	18,20	15,00	13,15	10,95
SN7495N	18,20	15,00	13,15	10,95
SN7496N	21,90	18,10	15,85	13,2
SN7497N	nog niet bekend			
SN74100N	29,40	24,30	21,30	17,70
SN74107N	8,75	7,20	6,30	5,25
SN74121N	9,55	7,89	6,90	5,75
SN74122N	13,50	11,20	9,80	8,15
SN74123N	32,80	27,10	23,80	19,80
SN74141N	22,80	18,80	16,45	13,70
SN74150N	37,50	31,00	27,20	22,60
SN74153N	13,30	10,95	9,60	7,99
SN74155N	12,35	10,20	8,95	7,45
SN74164N	33,50	27,70	24,30	20,20
SN74180N	18,35	15,15	13,25	11,05
SN74191N	49,00	40,50	35,50	29,55
SN74192N	37,00	30,60	26,80	22,30
SN74193N	37,00	30,60	26,80	22,30
SN74196N	19,50	16,10	14,10	11,75
SN74197N	19,50	16,10	14,10	11,75